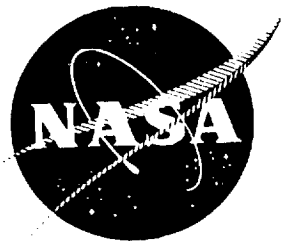

DEVELOPMENT OF ION IMPLANTATION TECHNIQUES FOR MICROELECTRONICS

By H.L. DUNLAP, R.G. HUNSPERGER, O.J. MARSH,

OCTOBER 1969

PREPARED UNDER CONTRACT NO. NAS 12-124 BY

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3011 MALIBU CANYON ROAD
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ELECTRONIC RESEARCH CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

FOREWORD

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DEVELOPMENT OF ION IMPLANTATION TECHNIQUES FOR MICROELECTRONICS

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I. SUMMARY

A. Silicon Carbide

We have produced SiC p-n junction diodes which operate very well between room temperature and 400°C. These are abrupt p-n junctions (when properly annealed) without the intrinsic layer observed in nearly all previous work.

We have shown that n-type layers can be made in p-SiC by implanting N, P, and Sb under much milder anneal conditions than those required for other doping techniques. P and Sb doping have not been achieved previously in SiC.

B. Gallium Arsenide

Several lines of evidence have shown that the intrinsic layer observed in implanted junctions arises from defects associated with As vacancies produced during implantation and annealing. We have demonstrated that the intrinsic region can be controlled or eliminated by the use of a SiO_x protective coating during implantation and annealing, and by implanting at room temperature.

We have measured the amount of lattice damage, as a function of dose, created when Cd is implanted in GaAs and have established the annealing behavior in the high and low dose regimes.

II. INTRODUCTION

We have investigated ion implantation and its development for use as a doping process in the fabrication of semiconductor devices in higher-bandgap materials. We have found that the ion implantation process can be used to fabricate excellent quality p-n junctions in GaAs and SiC.

In the previous interim contract report (October 1968) we presented the annealing requirements for Zn- and Cd-implanted layers in GaAs to obtain satisfactory electrical conduction. In addition, it was found that the junctions formed by implanting Zn or Cd into n-type GaAs resulted in p-i-n devices. The i region apparently was caused by the generation and diffusion of an unidentified defect species which formed deep trapping levels in the GaAs. We also reported that n-type conducting layers were formed in SiC after the implantation of Sb and Bi and subsequent annealing from 1000 to 1500°C. SiC etching techniques were of considerable importance because it had proved difficult to obtain good junction characteristics.

During this year we have emphasized the identification and elimination or control of the i region formation in implanted GaAs p-n junctions. The defects responsible for the semi-insulating "i" layer in GaAs appear to be related to vacancies generated by the escape of arsenic at the surface during implantation and annealing. The i layer has been controlled and eliminated by the introduction of process changes which prevent the dissociation and evaporation of arsenic. These changes include lowering the implant temperature or providing an SiO_x passivating layer before implantation.

Changing the implant temperature from 400°C to 23°C required an evaluation of the electrical behavior (by Hall effect) of the Zn- and Cd-implanted layers as a function of annealing conditions. Although this work is not yet complete, it is significant that p-type layers are formed after 30 min anneals at 120°C.

Ion-implanted GaAs diodes have been fabricated which behave as abrupt p-n junctions with measured breakdown voltages equal to the theoretically predicted values. Such diodes have been operated from 23° to 300°C. At 300°C the junctions were still definitely rectifying.

A study of lattice damage resulting from 60 keV Cd^+ ion implantation of GaAs substrates held at room temperature and damage annealing was begun this year, employing three techniques for measuring the damage: (1) Rutherford scattering measurements; (2) spectral reflectivity measurements; and (3) scanning electron microscope observations. Ion doses of greater than $10^{14}/cm^2$ appear to form an amorphous layer. Anneal of light implants ($\sim 4 \times 10^{13}/cm^2$) shows a significant anneal stage at 250 to 300°C, while heavier implants show little anneal up to 500°C.

It has been found necessary to SiO_x overcoat sulfur implants performed at 23°C prior to anneal in order to prevent apparent outdiffusion of the sulfur. With this precaution, n-type layers are formed after 800°C annealing.

The potential advantage of ion implantation over other device fabrication processes is best shown by the results obtained in the fabrication of SiC p-n junctions. The hexagonal form of SiC is normally grown at temperatures of 2500°C or above and the diffusions for forming junctions are normally carried out at 2000 to 2500°C. Grown p-n junctions have been formed at 1740°C by the traveling solvent method and at 1650°C by epitaxial growth from saturated silicon melts. These growth and diffusion processes typically require that the high temperature be maintained for hours.

In this report we discuss p-n junctions fabricated in p-type SiC by implanting nitrogen, phosphorus, or antimony and subsequently annealing at temperatures as low as 1000°C for 1 to 2 min. Optimum device characteristics have been obtained with 2 min anneals at 1400 to 1600°C.

The reverse characteristics of these junctions are of excellent quality and are somewhat better than those found in epitaxially grown junctions. The reverse current in one sample increased smoothly with applied voltage until an avalanche breakdown was observed at 46 V. Small "blue spots" are seen to appear at breakdown; they are located at etch pits which were present in the crystal prior to implantation. Photomultiplication is observed at bias voltages below breakdown with ultraviolet light incident on the junction area. The junctions showed excellent device characteristics at 400°C.

The nitrogen implants were made at room temperature and subsequently annealed to 1600°C for 2 min, resulting in n-type doped layers with carrier concentrations per square centimeter equal to approximately one-half the implanted dose, and an electron mobility of 30 $cm^2/V\text{-sec}$. Electron diffraction studies showed an amorphous layer after implant, and crystalline structure after 1500°C annealing. Similar results are found for P and Sb implants.

III. IMPLANTATION STUDIES IN GALLIUM ARSENIDE

A. Improvements in Processing and Fabrication Techniques

1. Polishing. — A machine has been constructed for polishing gallium arsenide and is now in operation. The machine, a modified version of that used by J.M. Whelan of USC, features combined mechanical and chemical etch polishing. The sample wafers are mounted on the face of a 4-in. diameter disk and are initially lapped flat. All abrasive is removed from the samples and holder by cleaning in solvents before they are placed on the polishing machine. The sample holder disk is then placed face down on the main wheel (12-in. diameter) of the polishing machine. This main wheel is covered with a polishing cloth which is kept saturated with a methyl alcohol-bromine etchant by a "dripper." The main wheel and the sample holder disk are driven to rotate so that the etchant is constantly agitated over the sample surface and etched material is swept away. The flatness and smoothness of the resulting surfaces are far superior to those obtained with earlier methods. Rutherford scattering measurements have shown that these polished surfaces are free of damage.

2. Implanted contacts. — We have previously reported (Ref. 1) that ohmic contact can be made to n-type GaAs layers without the formation of the usual surface barrier if a contact "pad" is formed by implantation of either sulfur or tin at room temperature. In order to establish whether this effect is a result of damage associated with the room temperature implantation or electrical activity of the tin and sultur atoms, a sample of n-type GaAs was implanted at room temperature with $1.1 \times 10^{16}/cm^2$, 30 kV argon ions. Argon has not been observed to be electrically active in GaAs, but such implants eliminated surface barriers of metals to these implanted surfaces. When gold probe contact probes were placed on the surface, ohmic contact was made; no surface barriers were observed from the I-V characteristics, and there was no evidence that a p-type layer had formed. Van der Pauw Hall measurements indicated a sheet resistivity of approximately 0.55 Ω/□, a mobility of 6700 $cm^2/V\text{-sec}$ (n-type), and a surface carrier concentration of $1.7 \times 10^{15}/cm^2$. These values agree with those which the manufacturer gives for the substrate material. Thus it

appears that ohmic contacts produced by room temperature implantation result from damage rather than electrical activity; it is likely that any ion can be used to produce such contacts, regardless of its expected electrical activity in GaAs.

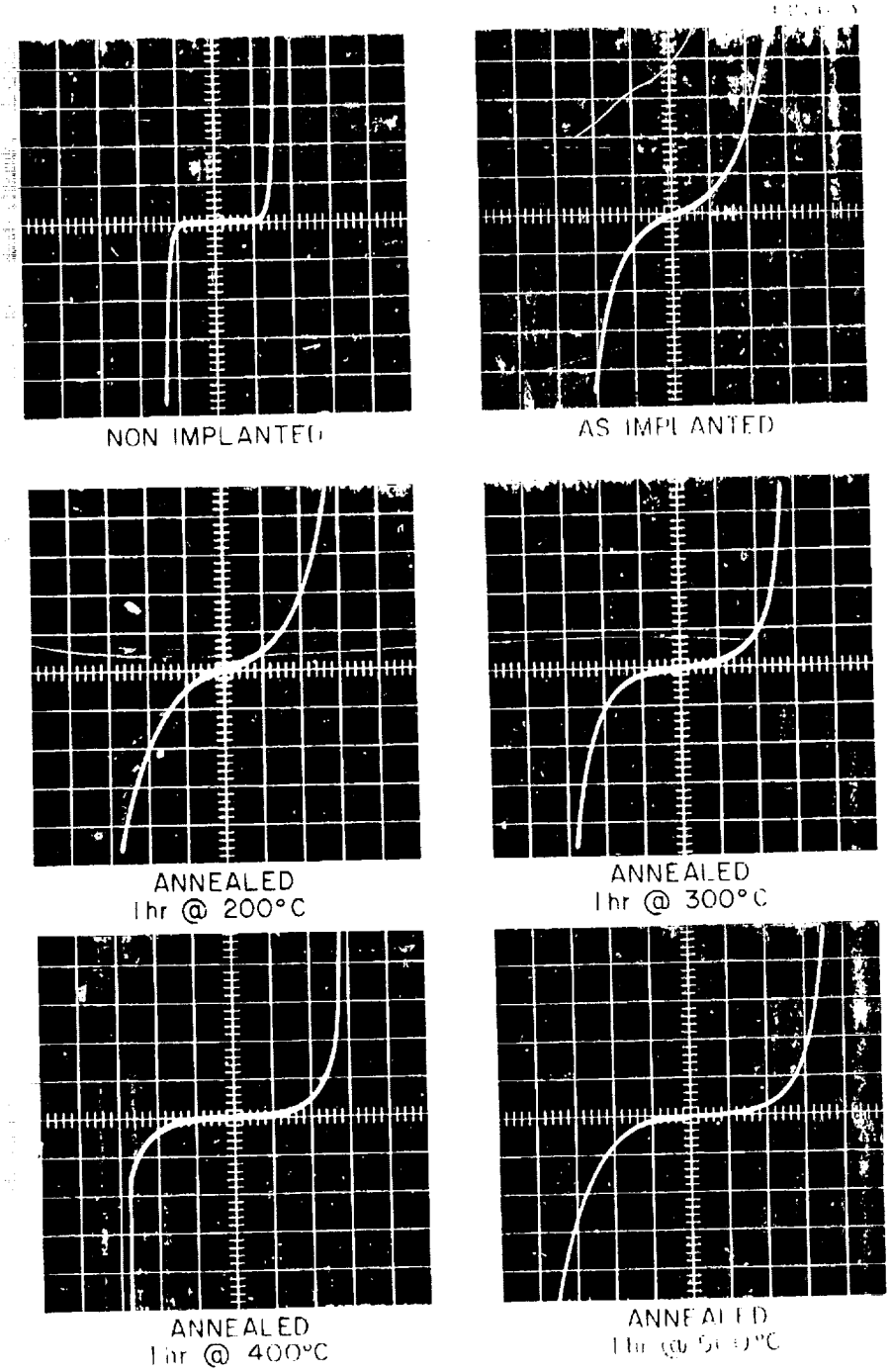
Various samples implanted as described were annealed for 1 hour at temperatures of 100, 200, 300, 400, and 500°C. The V-I characteristics measured between a pair of gold probe-point contacts to the implanted surface of these samples are shown in Fig. 1. It can be seen that the ohmic contacts were unaffected up to 200°C, but some nonlinear behavior was observed at 300°C. For samples annealed at 400 and 500°C, ohmic contact was no longer obtainable. Surface barriers formed when contact was attempted, as in non-implanted n-type GaAs. This indicates that the damage produced by the implant anneals at ~300°C, as observed in our Rutherford scattering work reported earlier (Ref. 1).

B. Damage Studies

A study of lattice damage resulting from 60 kV Cd^+ ion implantation of GaAs substrates was begun this year, with much of the work supported by company funds. Three independent damage measurement techniques have been employed: (1) Rutherford scattering measurements (in collaboration with E. Westmoreland, California Institute of Technology); (2) spectral reflectivity measurements (performed with G. Shifrin, HRL); and (3) scanning electron microscope observations (made in conjunction with E. Wolf, HRL (Ref. 2)). Damage was measured in a series of GaAs substrates implanted at room temperature with doses of 60 kV Cd^+ ions ranging from $1 \times 10^{12}/cm^2$ to $1 \times 10^{15}/cm^2$.* The acquisition and analysis of data from these experiments are not yet complete, but at present it can be stated that the results obtained with the three different damage measurements techniques are in qualitative agreement. The Rutherford scattering data shown in Fig. 2 indicate that relatively little damage† results in samples implanted with a dose of $3 \times 10^{12}/cm^2$,

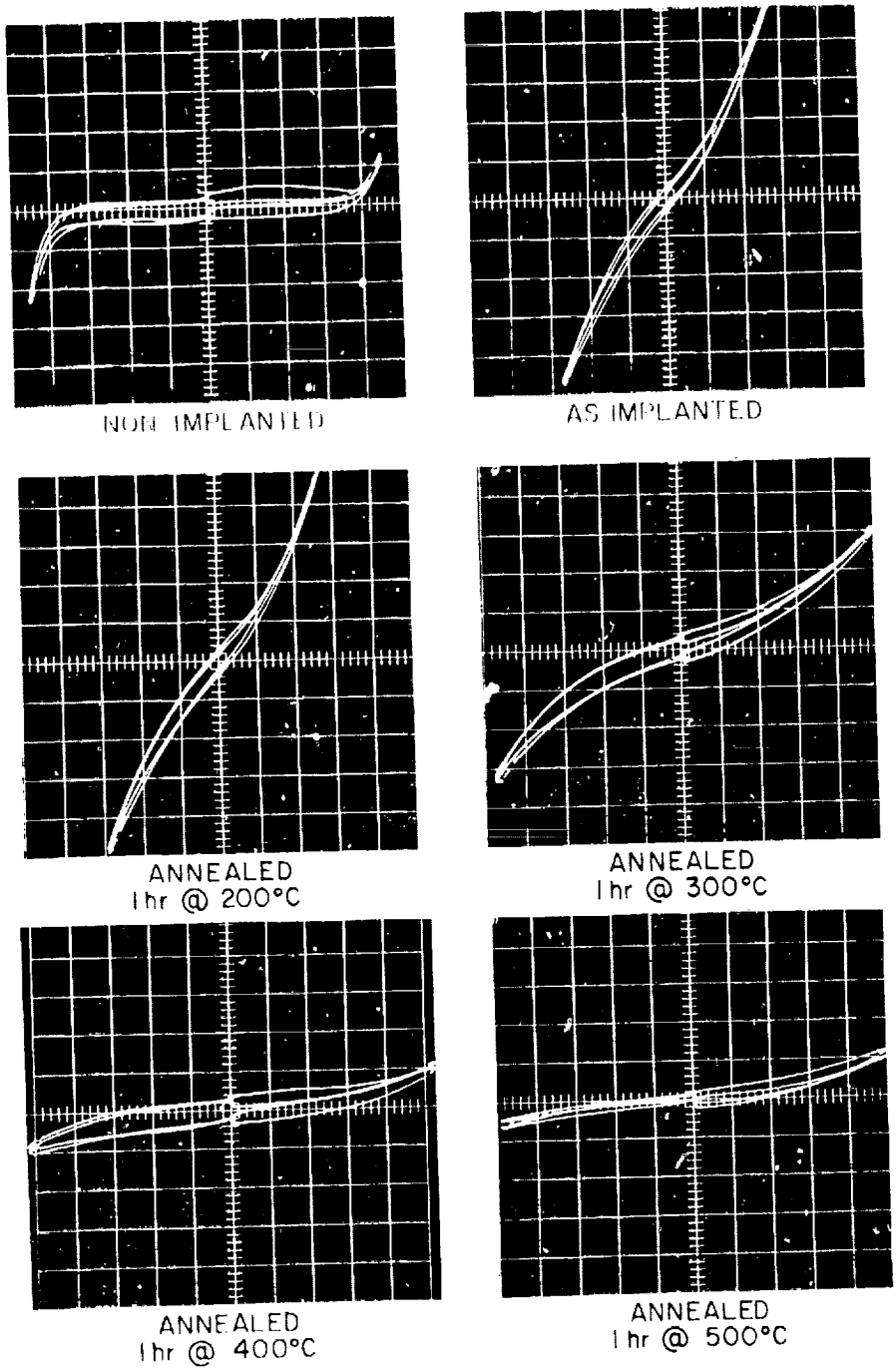
*These ion doses have been corrected for error introduced by secondary electron emission during implant; they are about a factor of three smaller than the values measured without secondary electron suppression.

†The damage scale shown in Fig. 2 is arbitrary, and shows the fractional amount of lattice disorder relative to that in a sample implanted with a dose of $10^{15}/cm^2$. The implanted layer in that sample is assumed to be totally disordered or amorphous.



(a)

Fig. 1. Current [illegible] voltage characteristics [illegible] pair of gold probe points [illegible] room temperature [illegible] non-implanted [illegible].


NON IMPLANTED
AS IMPLANTED
ANNEALED
1 hr @ 200°C
ANNEALED
1 hr @ 300°C
ANNEALED
1 hr @ 400°C
ANNEALED
1 hr @ 500°C
VERTICAL = 1μA/DIV
HORIZONTAL = 1 V/DIV

(b)

Fig. 1 (Cont'd).

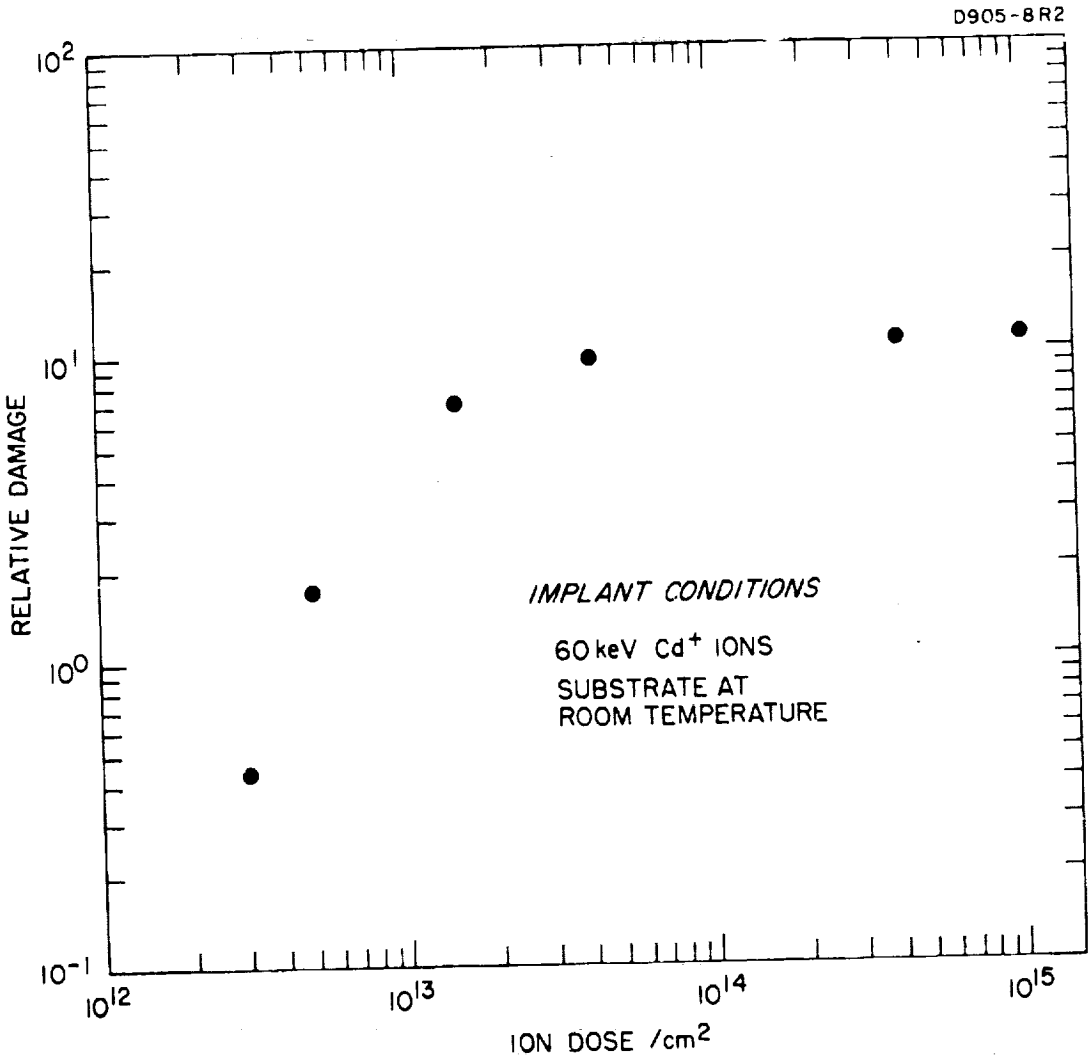


Fig. 2. Damage versus dose for cadmium-implanted GaAs as measured by 1 MeV He channeling.

while the surface is essentially totally disordered for samples implanted with $10^{15}/cm^2$ or higher. Very heavy damage is present in samples with doses $\geq 4 \times 10^{12}/cm^2$. Spectral reflectivity measurements show that reflectivity at 2450 Å is unchanged by a dose of $1 \times 10^{12}/cm^2$; however, it decreases more or less uniformly with increasing dose up to $\sim 5 \times 10^{13}/cm^2$, at which point the reflectivity versus dose curve begins to level off (see Fig. 3). The change in reflectivity at 4250 Å is not as great as that at 2450 Å, and no distinct break-point can be determined. Figure 3 shows the change in reflectivity at only two of the key peaks of the spectrum of GaAs shown in Fig. 4, but reflectivity was observed to decrease over the entire spectrum as ion dose was increased. The electron scattering patterns obtained with the scanning electron microscope are also in qualitative agreement with these results, showing essentially an undamaged crystalline structure for a dose of $1 \times 10^{12}/cm^2$ and a structureless amorphous layer in a $10^{15}/cm^2$ implanted sample. Heavy damage caused almost complete destruction of the crystalline pattern, even in a sample implanted with a dose of $10^{14}/cm^2$. (Figure 5 shows typical SEM photographs.) No technique has yet been developed for the quantitative analysis of the scanning electron microscope data to determine relative lattice disorder.

The anneal behavior of lattice damage has been studied in some of these samples of 60 kV cadmium (room temperature) implanted GaAs. Spectral reflectivity was measured as a function of anneal temperature for two samples with doses of $\sim 4 \times 10^{13}/cm^2$ and $\sim 1 \times 10^{15}/cm^2$. The samples were annealed for 10 min periods at temperatures from 50 to 500°C (50°C steps), and their spectral reflectivity was measured after each step. The reflectivity of the smaller-dose implant increased sharply after anneal at 250°C, approaching that of a nonimplanted sample, while that of the heavier implant showed a generally upward trend above 300°C. However, even after 500°C anneal the reflectivity remained far below that of undamaged samples (see Fig. 6). The interpretation of the reflectivity data was greatly complicated by excessive "scatter" of the points, resulting from a reflecting surface orientation dependence of the reflectivity measurement; however, the "break" in the curves at 250°C and 300°C, respectively, is clearly discernible. It was determined later that the orientation dependence of the reflectivity was caused by misalignment of the front surface of the sample with respect to the light beam. The samples were mounted with their back surface flush against a reference plane, but the front and back surfaces of the samples were significantly nonparallel. This problem will be avoided in future measurements by aligning samples with respect to the front surface. (A new set of

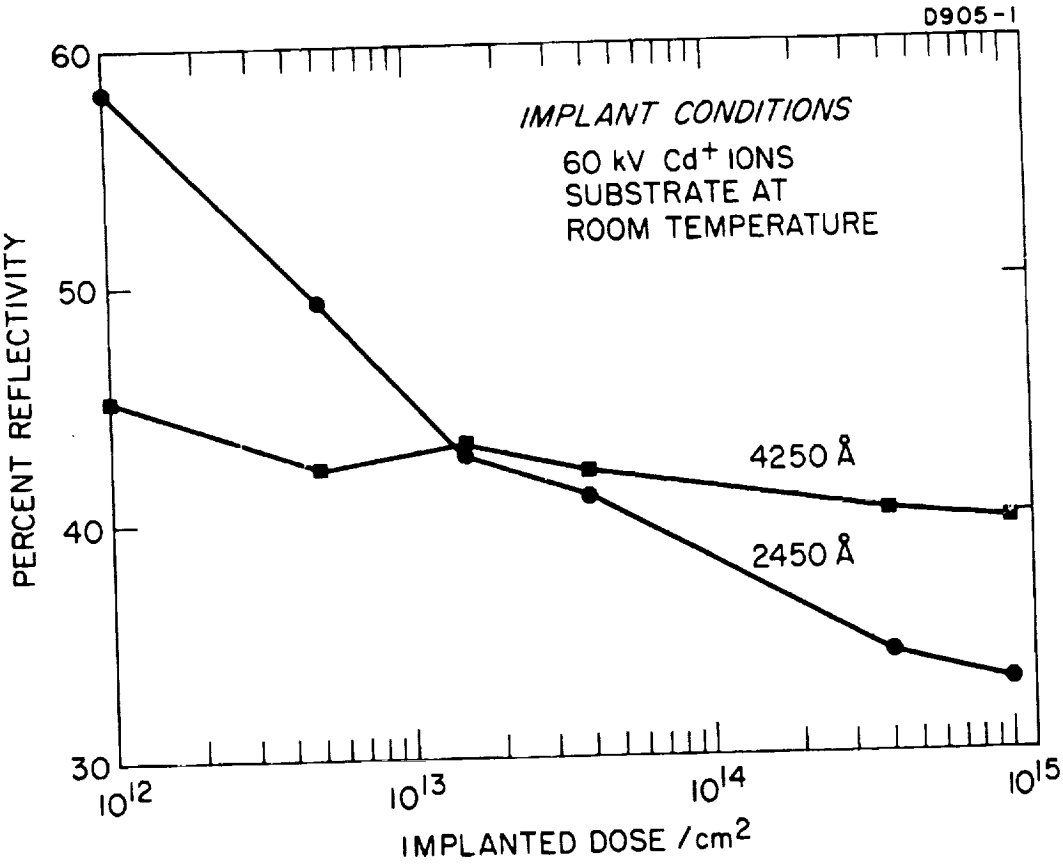


Fig. 3. Reflectivity versus ion dose (measured at two different wavelengths).

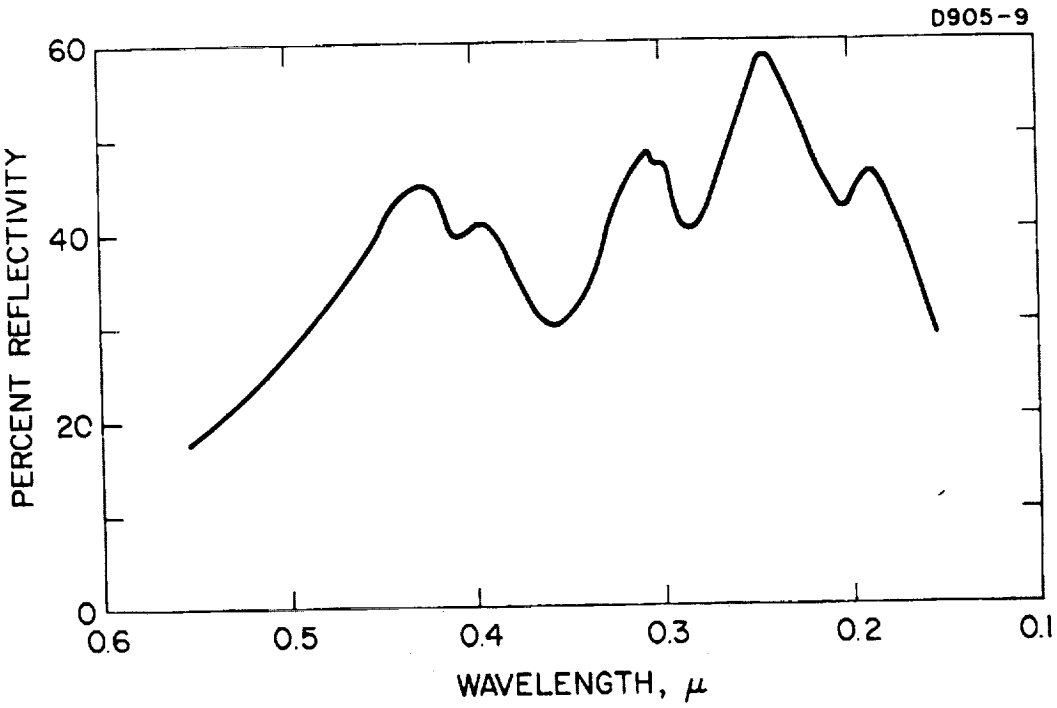


Fig. 4. Reflectivity spectrum of undamaged (crystalline) GaAs.

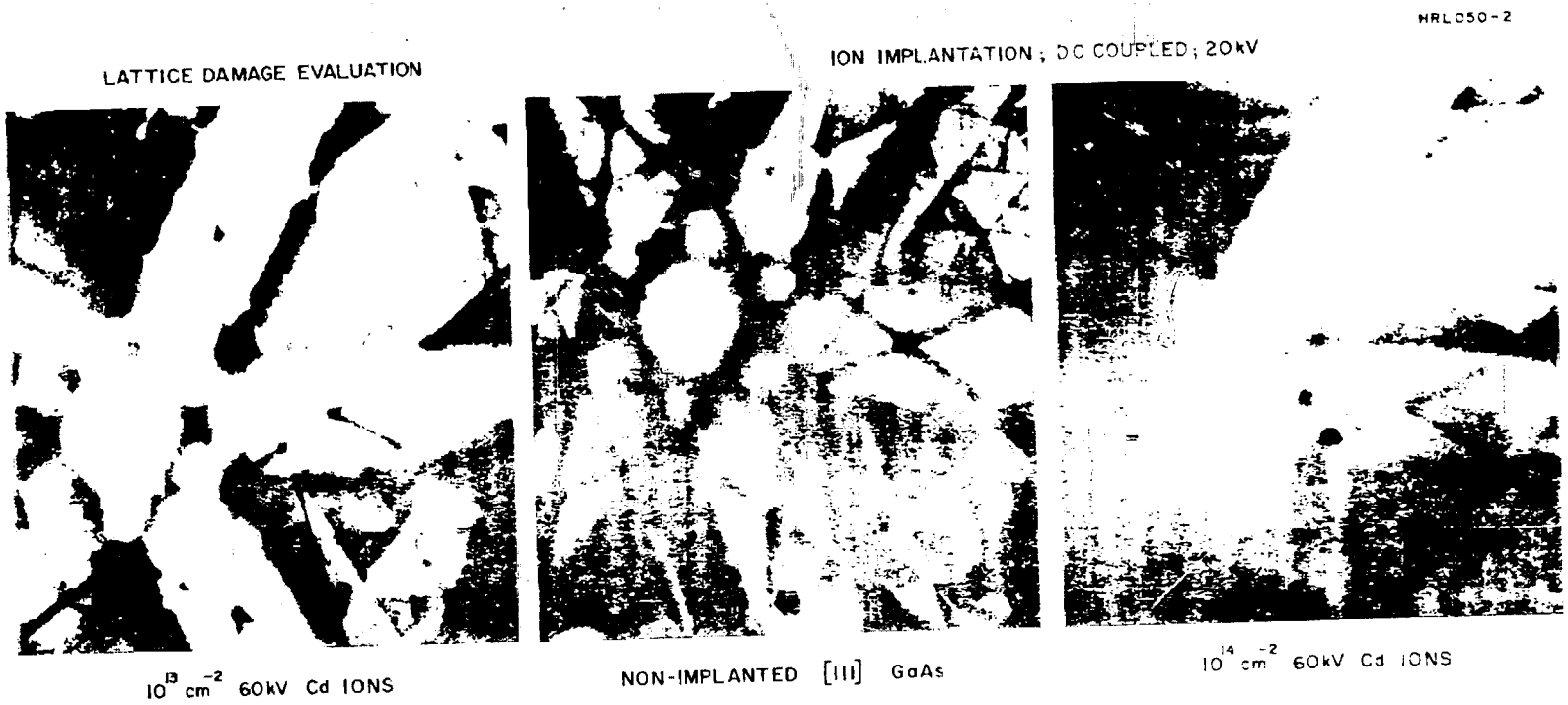


Fig. 5. Scanning electron microscope pseudo-kikuchi patterns for 60 keV Cd implanted GaAs.

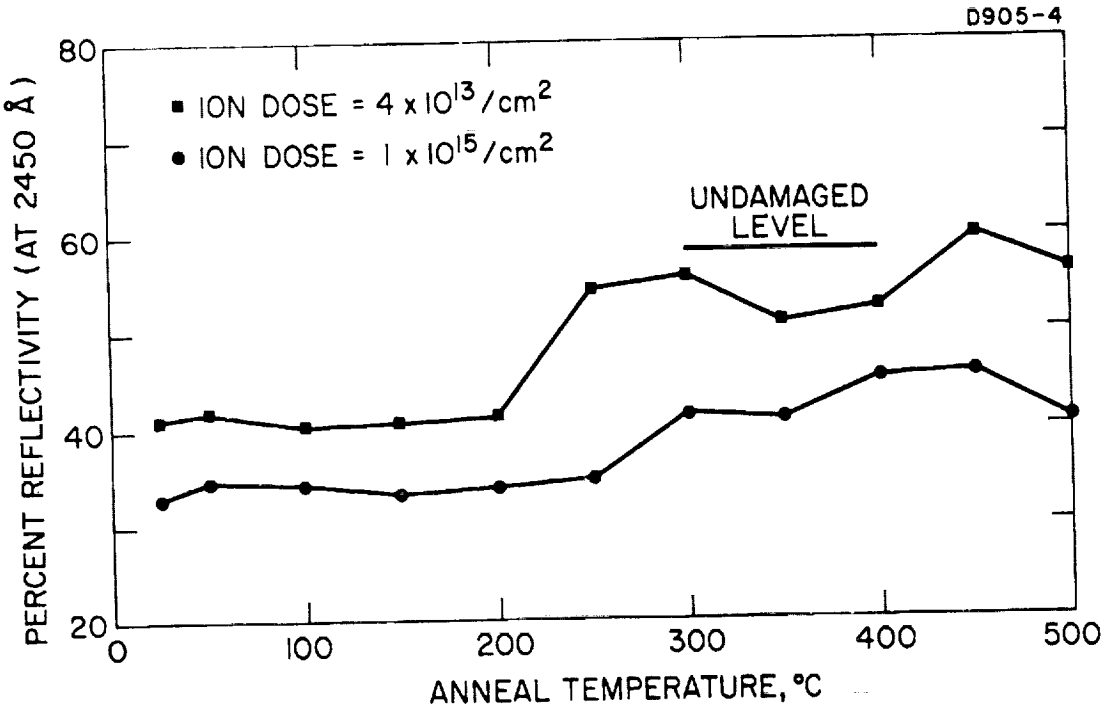


Fig. 6. Change in reflectivity of GaAs resulting from annealing (10 min anneal periods).

n-type substrates has been cut and polished, and is presently being implanted with 60 keV Cd^+ ions at room temperature. The samples will be used first for a detailed measurement of damage versus ion dose and anneal behavior, using the spectral reflectivity method. Hall measurements then will be made to correlate the results with electrical characteristics of the implanted layer.) The damage annealing results of spectral reflectivity measurements are in reasonably good agreement with damage measurements made by the Rutherford scattering method. These show a sharp anneal step below 250°C for the $4 \times 10^{13}/cm^2$ dose sample and a gradual, partial anneal of damage in the $1 \times 10^{15}/cm^2$ sample.

For heavy implants, which create a totally amorphous layer in the crystal, it appears that annealing above 500°C is required to completely heal the damage caused by implantation. The damage from relatively light implants ($<10^{14}/cm^2$), which is thought to consist of isolated damage clusters, anneals almost completely at temperatures below 500°C.

The Scanning Electron Microscope is also being used at present for the study of damage annealing in these 60 kV cadmium implanted samples. Very few data have been collected as yet, but the initial results indicate a substantial anneal step between 200 and 300°C for lightly implanted samples.

C. Electrical Properties of Room-Temperature-Implanted Layers

1. Sulfur implants. — Sulfur was implanted into high resistivity p-type GaAs substrates at room temperature using energies of 30 and 60 keV and doses from $1.8 \times 10^{13}/cm^2$ to $1.25 \times 10^{15}/cm^2$. Following implantation, all samples exhibited n-type layers; however, the layers were of high resistivity, as described in a previous report (Ref. 1). No surface barriers developed when contact was made to the samples with gold probes; ohmic contact was made. The samples were encapsulated in SiO_2 in preparation for high-temperature annealing. After the encapsulation process, which involved heating the samples to 480°C for 2 hours, it was found that the n-type layer was no longer present in any sample. Thermal probe measurements indicated p-type material. Subsequent annealing for 10-min periods from 600°C to 900°C in 100°C steps produced no n-type layer formation, except in a sample implanted at 30 kV with a dose of $2.5 \times 10^{14}/cm^2$.

anneal at 900°C. (The conductivity was less than that of the as-implanted layer). It is possible that the loss of electrical activity in the annealed samples resulted from outdiffusion of sulfur atoms during the encapsulation process, before the SiO_2 layer had become thick enough to retard outdiffusion. Sulfur diffuses fairly rapidly in GaAs and has a vapor pressure approaching 1 atm at 480°C; hence it is conceivable that it could diffuse to the surface and evaporate, leaving no observable layer. This hypothesis is supported by the fact that p-n junction diodes have been formed by implanting sulfur ions through an oxide into p-type substrates and subsequently annealing at 800°C without removing the oxide. (See Section III-E.)

We have considered the possibility that the n-type layers produced by room temperature implantation of sulfur ions (as described above) might be the result of implantation damage rather than electrical activity of the sulfur atoms. However, this does not appear to be the case, since a substrate of p-type GaAs implanted with $1.1 \times 10^{16}/cm^2$, 30 kV argon ions at room temperature gave no indication of an n-type layer. Room temperature implantations of tin ions also fail to produce the n-type layers which have been observed for the sulfur implantations.

2. Zinc implants. — During this year we began the measurement of the electrical properties of room-temperature zinc-implanted samples as a function of annealing. Samples implanted with doses of $10^{13}/cm^2$ to $10^{16}/cm^2$ 20 kV ions did not appear to have a p-type layer in the "as implanted" condition; after anneal at 120°C for 30 min a p-type layer did appear. Measurements of the V-I curves indicated that a rectifying junction was present between the implanted layer and the substrate; however, the resistivity of this layer was very high. For example, van der Pauw Hall measurements on the $10^{15}/cm^2$ dose sample showed sheet resistivity $\approx 10^5$ Ω/□, mobility ≈ 3 cm^2/V sec, and surface carrier concentration $\approx 2.5 \times 10^{13}/cm^2$. It was not possible to measure the corresponding values for the sample containing the $10^{13}/cm^2$ dose because the layer resistivity was too high. The change in resistivity as a function of anneal temperature for these samples is shown in Fig. 7; mobility and carrier concentration data are given in Fig. 8. The surface of the samples was protected during anneal by using the cover wafer technique at temperatures up to 500°C, and a pyrolytically deposited SiO_2 film was used for anneals above 500°C. Layer resistivity remained above 10^4 Ω/□ for all but the $10^{16}/cm^2$ dose sample, even after annealing at

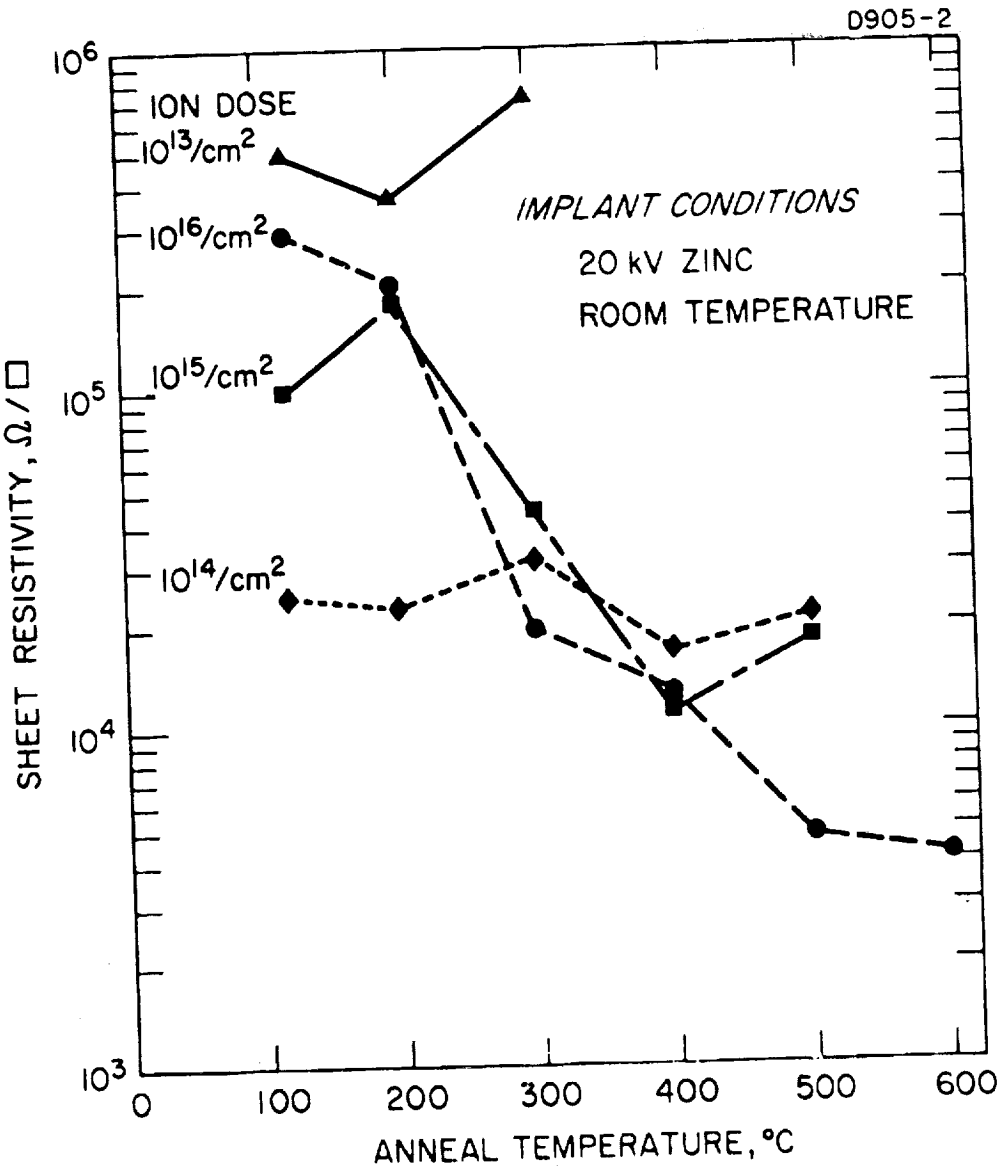


Fig. 7. Dependence of GaAs resistivity on anneal temperature (10 min anneal periods).

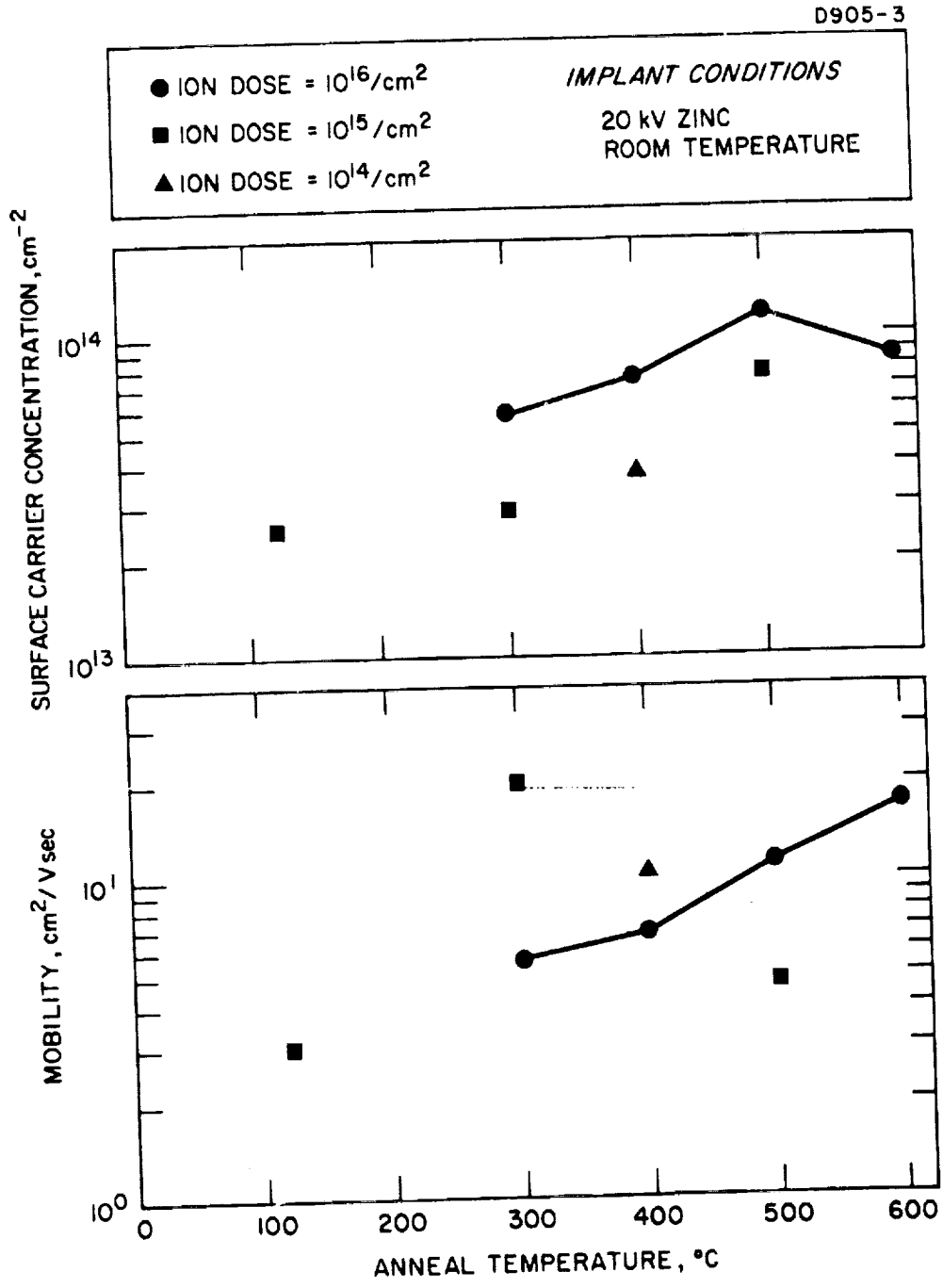


Fig. 8. Dependence of mobility and carrier concentration on anneal temperature of implanted GaAs (10 min anneal periods).

500°C. This high resistivity was a result of low mobility and low carrier concentration. The resistivity of all of the implanted layers was sufficiently high that accurate measurements of mobility and carrier concentration were difficult and in some cases impossible; hence the data of Fig. 8 exhibit a great deal of scatter, except for the $10^{16}/cm^2$ sample. Nevertheless, it is significant that a p-type layer was formed in all of these room-temperature implanted samples after only a 120°C, 30 min anneal. Our previous work has shown that samples implanted with 20 kV Zn^+ ions at 400°C require annealing at 500°C or above in order to form even a high-resistivity p-type layer.

It is also interesting to note that the resistivity of the sample implanted with a $10^{16}/cm^2$ dose showed a significant anneal step between 200 and 300°C. Damage studies, described in Section II-B, have indicated an anneal step in this temperature range.

D. Junction Depth Measurements

Angle section and stain techniques have been used to measure junction depth in samples of GaAs implanted with approximately $1 \times 10^{16}/cm^2$, 20 kV zinc ions at 400°C. An etchant of 1 part HNO_3 to 6 parts H_2O_2 was used for staining. Substrates (n-type) doped from $5 \times 10^{15}/cm^3$ to $1.8 \times 10^{18}/cm^3$ were used, but junction depth appeared to be independent of substrate impurity concentration. The $1.8 \times 10^{18}/cm^3$ doped substrate yielded the clearest stain pattern; the junction was frequently difficult to observe in high resistivity substrate material. Figure 9 shows the junction in a sample of $1.8 \times 10^{18}/cm^3$ substrate material, implanted as above after anneal at 900°C for 35 min. The junction depth in this case is 0.44 μ. The surface of the sample is at the top of the figure, and the angle-lapped bevel is in the lower portion. Note that the junction depth is quite uniform, except for a short-range ripple caused by irregularity of the polished surface. (The chemical-mechanical polishing machine described in Section III-A had not been completed at the time this sample was prepared; hence it was merely chemically polished in a beaker.) Junction depth was measured as a function of anneal time at 800 and 900°C; the results are shown in Fig. 10. As a result of zinc diffusion, the junction depth changed from about 1000 Å immediately after implantation to 1.3 μ after anneal at 900°C for 5 hours. It is very difficult to measure junction depth

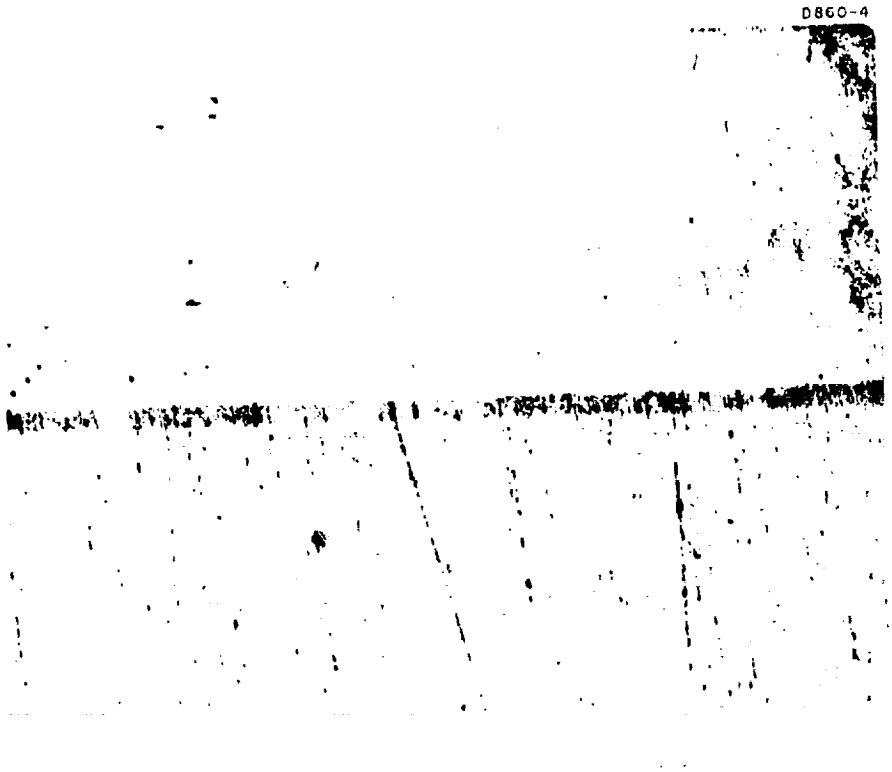


Fig. 9. Angle sectioned and stained sample of zinc-implanted GaAs. The dark band is the p-type implanted layer.

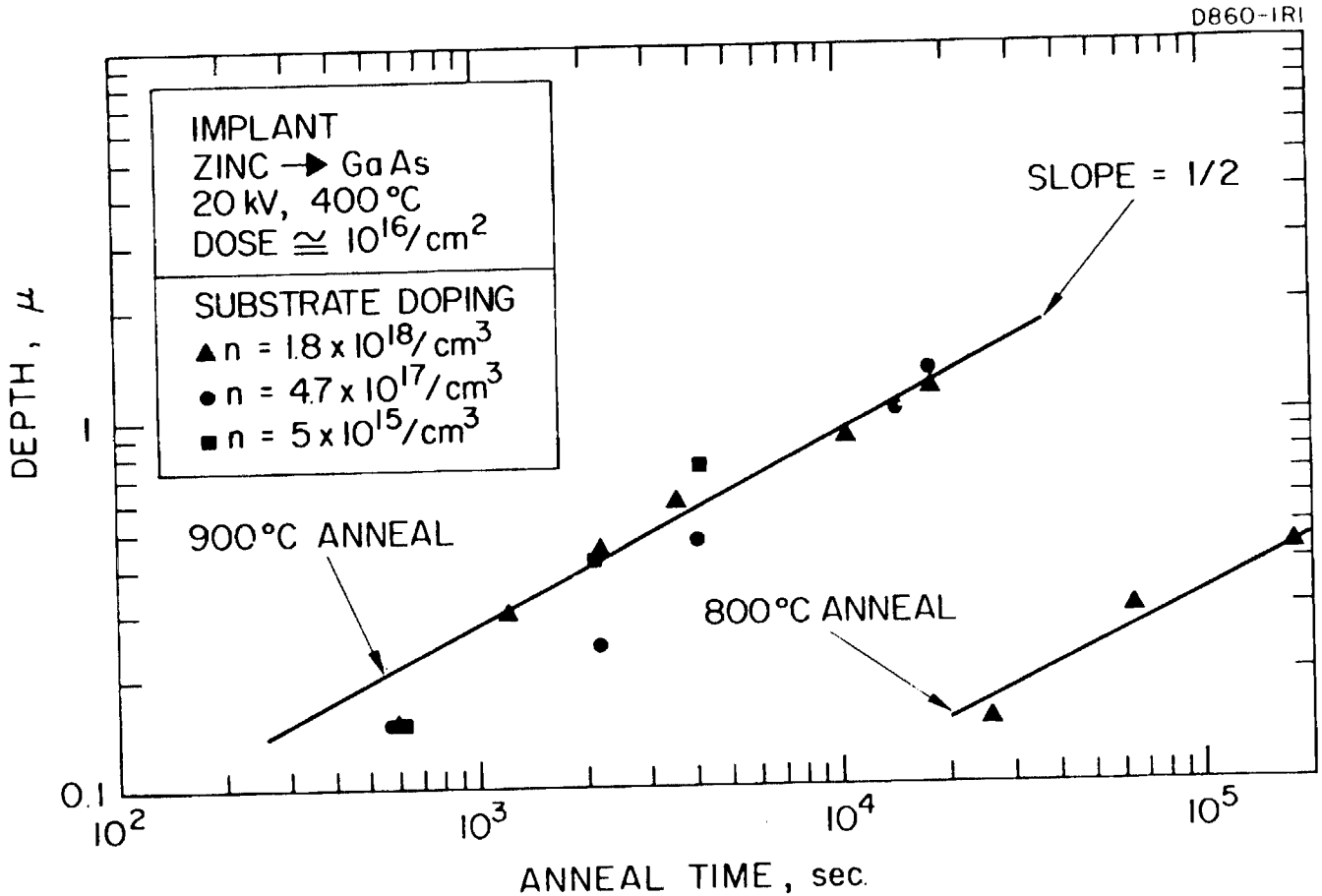


Fig. 10. Dependence of junction depth on anneal conditions for Zn-implanted GaAs.

for brief anneal periods because of poor staining; more effort must be devoted to accurate measurement of the "as-implanted" junction depth. Annealing at 800°C also produced measurable change in junction depth, reaching 0.44 μ after 50 hours. At both temperatures the depth was proportional to $(\text{time})^{1/2}$, as would be expected from diffusion theory; in all cases, however, the depths were much less than would be expected for diffusion from a constant-concentration zinc source in the same time interval. Dispersion of the originally implanted atoms by diffusion results in reduction of the diffusion coefficient, which is highly concentration-dependent for zinc in GaAs. It is probably this effect which causes the change of junction depth during anneal to be smaller than expected from published observations of zinc diffusion from a constant-concentration source (Ref. 3).

We have also had some success in staining n-type layers produced by tin implantation. The etch used was (by weight) 1 part $K_3Fe(CN)_6$:1 part KOH:40 parts H_2O, which stains the p-type substrate dark, revealing the section of the n-type layer as a white "band." A sample implanted with $\approx 1 \times 10^{16}/cm^2$, 35 kV Sn^+ ions at 400°C and annealed for 2 hours at 900°C had a junction depth of 0.44 μ. For comparison, a 20 kV zinc implant annealed for 2 hours at 900°C has a junction depth of 0.8 μ.

E. Implanted Diodes

The effort to produce good quality diodes by ion implantation has been intensified during this year, with the work being concentrated on room-temperature implants. The cause of the previously reported semi-insulating layer in implanted diodes has been tentatively identified, and effective methods of eliminating the i layer (when so desired) have been developed. Recent results, described in Section II-F, indicate that the defects responsible for the i layer are probably related to vacancies generated by the escape of arsenic at the surface during implantation and annealing. When steps are taken to prevent this dissociation, diodes are formed which have either no i layer or a much reduced i layer thickness.

The diodes which we described in earlier reports were created by implantation of substrates at 400 and 500°C. In order to determine the effect of room temperature implantation on diode operating characteristics, a set of diodes was fabricated by implanting nonheated substrates with both 20 kV and 84 kV Zn^+ ions in doses ranging from 10^{13} to $10^{16}/cm^2$. Following implantation , the substrates were coated with SiO_2 by pyrolytic decomposition of tetraethylorthosilicate and were annealed at 650°C for 3 hours. After anneal, diode "mesas" about 0.5 mm in diameter were formed by masking and methyl alcohol-bromine etching the substrates. Contact was made to the n-type substrates by alloying with nickel-tin. Electrical connections were made using gold probe pressure contacts, and the diode V-I characteristics were observed on a curve tracer. The diodes had reverse breakdown voltages ranging from 30 to 120 V, with the high breakdown voltages being observed in the $10^{16}/cm^2$ dose samples. The $10^{13}/cm^2$ samples had no observable junction formation. The forward resistance of all of the diodes was somewhat high (in the 10^3 - 10^4 Ω range), probably because of the high substrate resistivity and the presence of a semi-insulating layer in the junction region. Figure 11 shows the V-I characteristics of one of the better diodes of this set.

In an effort to obtain diodes of lower forward resistance than that of the above devices, a set of diodes was made by implanting $1 \times 10^{16}/cm^2$, 20 kV, Zn^+ ions into heavily doped ($n = 1.8 \times 10^{18}/cm^3$) n-type substrate material and annealing for 10 min at various temperatures from 500 to 900°C. Those diodes annealed below 700°C had forward resistances on the order of 100 Ω and reverse breakdown voltage ~8 V; those annealed at 700°C and above had forward resistances of 10 to 30 Ω and reverse breakdown voltage ~6 V. These breakdown voltages approximate the theoretical value calculated by Sze and Gibbons (Ref. 4) for an abrupt junction in GaAs (~6 V for a substrate background doping of $1 \times 10^{18}/cm^3$). C-V measurements indicated that the sample annealed at 500°C had a relatively thin semi-insulating layer (0.166 μ) present in the junction, and that the i layer thickness was even less in the 600 and 700°C annealed sample. The 800 and 900°C samples had no measurable i layer and were abrupt p-n junction diodes. The decrease in i layer thickness to zero with increasing anneal temperature contrasts with the behavior of zinc implants at 400°C into lightly doped substrate material, in which anneal at higher temperature produced thicker i layers; this effect is described in detail in Section III-F.

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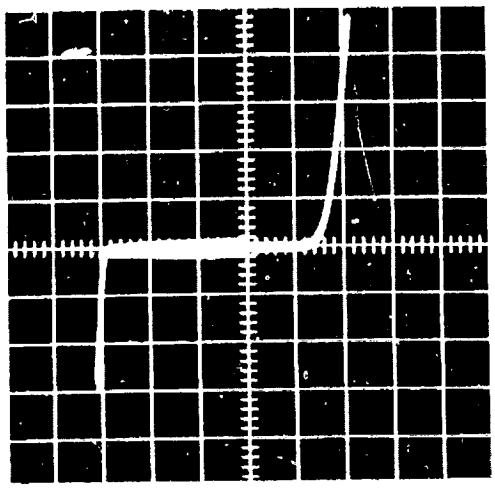

VERTICAL SCALE = 10 μA/DIV
HORIZONTAL SCALE = 0.5 V/DIV (FORWARD)
= 10 V/DIV (REVERSE)

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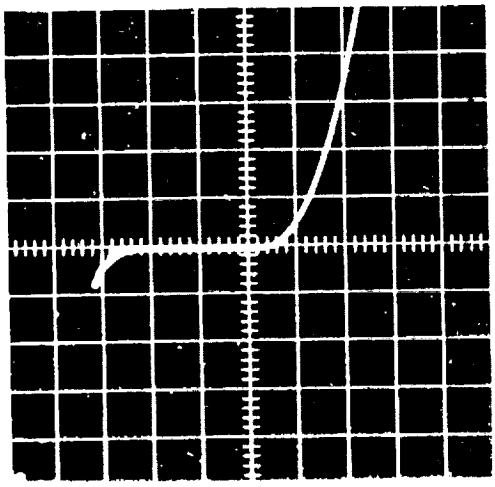


VERTICAL SCALE = 100 μA/DIV
HORIZONTAL SCALE = 2 V/DIV (FORWARD)
= 10 V/DIV (REVERSE)

Fig. 11.
V-I characteristics of a zinc-implanted GaAs diode.

A third set of diodes was made by implanting 1.2 x $10^{15}/cm^2$, 60 kV, Cd^+ ions into moderately doped (n = 1.5 x $10^{17}/cm^3$) n-type substrate material. Anneal of these samples for 10 min periods at temperatures from 600 to 800°C produced diodes with reverse breakdown voltage ~30 V and forward resistance on the order of 100 Ω. In general the 700°C annealed diodes appeared to have the highest breakdown voltage and lowest leakage current and forward resistance. C-V measurements indicated a much thinner semi-insulating layer in these room temperature implanted diodes than was observed in 400°C implanted cadmium diodes.

Having obtained relatively good room-temperature operating characteristics for some implanted diodes, we have initiated measurement of the high temperature operating characteristics of ion-implanted GaAs diodes. A hot stage has been built which permits measurement of the V-I characteristic and capacitance versus voltage variation of a p-n junction diode as a function of temperature up to 300°C. A pressure contact to the implanted layer of the diode is made by means of a gold probe, while the substrate is contacted through the carbon block of the heating stage. For an n-type substrate, an alloyed Sn-Ni ohmic contact is made to the undersurface of the GaAs substrate so that there is no surface barrier between the substrate and the carbon block. Using this setup in conjunction with a curve-tracer-oscilloscope, we have observed the V-I curve of a diode made by implanting a dose of 1 x $10^{15}/cm^2$, 84 keV zinc ions, at room temperature, into an n-type substrate with n = 5 x $10^{15}/cm^3$. After implantation the diode was coated with sputtered SiO_2 and annealed at 650°C for 3 hours. At room temperature this diode had a reverse breakdown voltage of V_B ~ 25 V and a forward resistance of 2000 Ω; the reverse leakage current was less than 1 μA. The relatively high forward resistance probably resulted from the small area of the gold probe contact to the implanted layer, and from a semi-insulating layer which was present in this diode. At 100°C there was no significant change in the V-I curve (see Fig. 12). At 200°C the reverse breakdown voltage dropped to about 22 V, and the leakage current at 1/2 V_B was 5 μA. At 300°C the junction was still definitely rectifying, but V_B had decreased to 20 V and the leakage current at 1/2 V_B was approximately 60 μA. These initial results of operating an ion-implanted GaAs diode at elevated temperature are very encouraging; we intend to continue the work, measuring detailed point-by-point V-I curves, and extending the measurements to the temperature which proves to be the upper limit

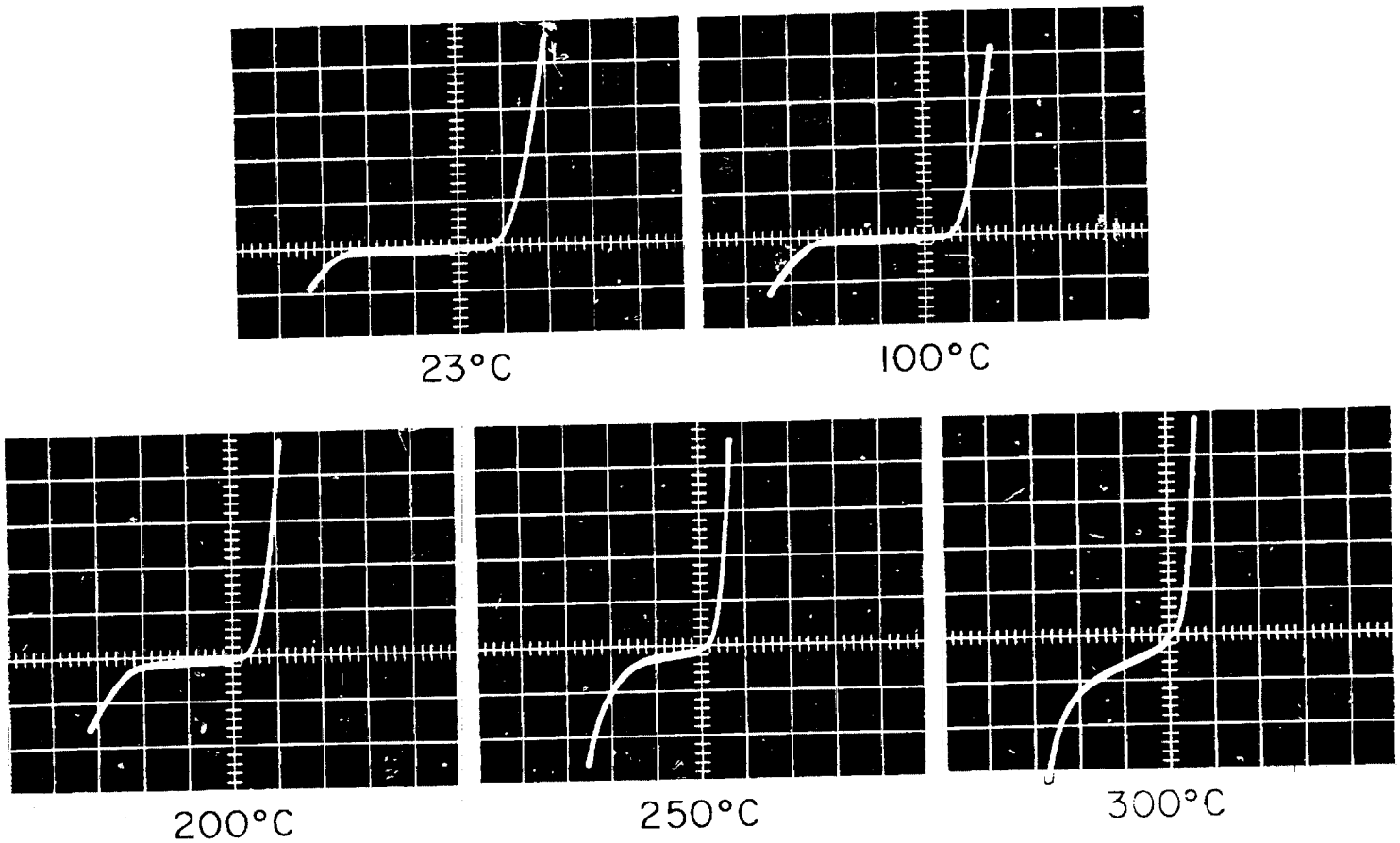


Fig. 12. Temperature dependence of the V-I characteristic of a zinc-implanted GaAs diode.

for operation of these diodes. A suitable oven, with an inert atmosphere, is now being constructed. We shall also determine whether there is any degradation when these diodes are operated at elevated temperature for extended periods of time.

Most of the implanted diodes we have studied were made by implanting p-type dopants (zinc or cadmium) into n-type substrates; however, we have recently begun examining some diodes made by implantation of an n-type dopant, sulfur. Three implantations of 85 keV sulfur ions into p-type substrates were performed at room temperature. The implants were made through a 700 Å oxide which had been sputtered onto the substrates at room temperature. The doses used were $1 \times 10^{14}/cm^2$, $1.2 \times 10^{15}/cm^2$, and $5 \times 10^{15}/cm^2$. Portions of each of the implanted samples were annealed at 800°C for 15 min, with the oxide still in place. This annealing resulted in the formation of a definite p-n junction in the two samples with dose $>10^{15}/cm^2$. Relatively strong light sensitivity was observed when the junctions were reverse biased. Thermal probe measurements also indicated n-type electrical activity in the implanted layer. To date only the reverse bias characteristics of these diodes have been observed; the formation of surface barriers at the gold probe contacts to the n-type implanted layer prevented measurement of the forward characteristics. Suitable contacts will have to be formed on these samples to allow measurement of the forward V-I characteristics. The successful creation of an n-type layer by sulfur implantation in these oxide coated samples is in marked contrast to the failure of similar attempts in uncoated samples. It is possible that the oxide is required to prevent outdiffusion of the sulfur atoms.

F. Investigation of the Semi-Insulating Layer in Implanted Diodes

Our previous work (Ref. 1) has shown that a semi-insulating layer often is observed in ion-implanted junctions. The thickness of the layer has been found to depend on both implantation and anneal conditions. The results described below indicate that the defects responsible for the semi-insulating layer appear to be related to vacancies generated by the escape of arsenic at the surface during implantation and annealing. When steps are taken to prevent this dissociation, diodes are formed which have either no i layer or a much reduced i layer thickness.

The thickness of the semi-insulating region was measured (using the C-V measurement technique, Ref. 1) for a number of implanted diodes which had been annealed for 10 min at temperatures up to 900°C. Figure 13 shows the results for zinc and cadmium implants at 400°C into a very lightly doped substrate ($n \approx 1.2 \times 10^{14}/cm^3$). A relatively thick semi-insulating layer was present in diodes annealed at 600°C, and the layer was even thicker in diodes annealed at higher temperature. Semi-insulating layers with thicknesses on the order of tens of microns or greater were observed only in diodes formed in very lightly doped substrate material. Our earlier work (Ref. 5) has shown that the i layer thickness varies approximately as the inverse square root of the substrate impurity concentration, for a fixed set of implantation and anneal conditions. The formation of the semi-insulating layer in the junction and the subsequent variation of thickness with annealing are believed to be caused by defects created during the implantation and subsequent anneal, which produce compensation to the depth where the concentration of defects equals the substrate impurity concentration. During anneal, localized defects (thought to be arsenic vacancies) produced by ion bombardment may diffuse through the lattice to form more complex and stable defects at far greater depths than the projected range of the implanted ions.

The anneal behavior of the semi-insulating layer in diodes implanted with the substrates held at room temperature instead of 400°C is shown in Fig. 14. The significant feature of the data is that the thickness of the semi-insulating layer decreased with increasing anneal temperature, and the diodes annealed at 800°C or 900°C had only a very thin i layer or none at all. The decrease of i layer thickness with increasing anneal temperature, which contrasts with the behavior of the 400°C implanted diodes, is thought to result partly from reduced vacancy generation during implantation; the resulting smaller number of deep-level compensating defects was unable to provide the concentration required for total compensation to greater depth when defect diffusion occurred.

The larger background impurity concentration of the substrates used for these samples also contributed to the decrease in i layer thickness by decreasing the depth to which total compensation could occur before the supply of defects was exhausted. In diodes made by room temperature ion implantation into heavily doped substrates, as shown

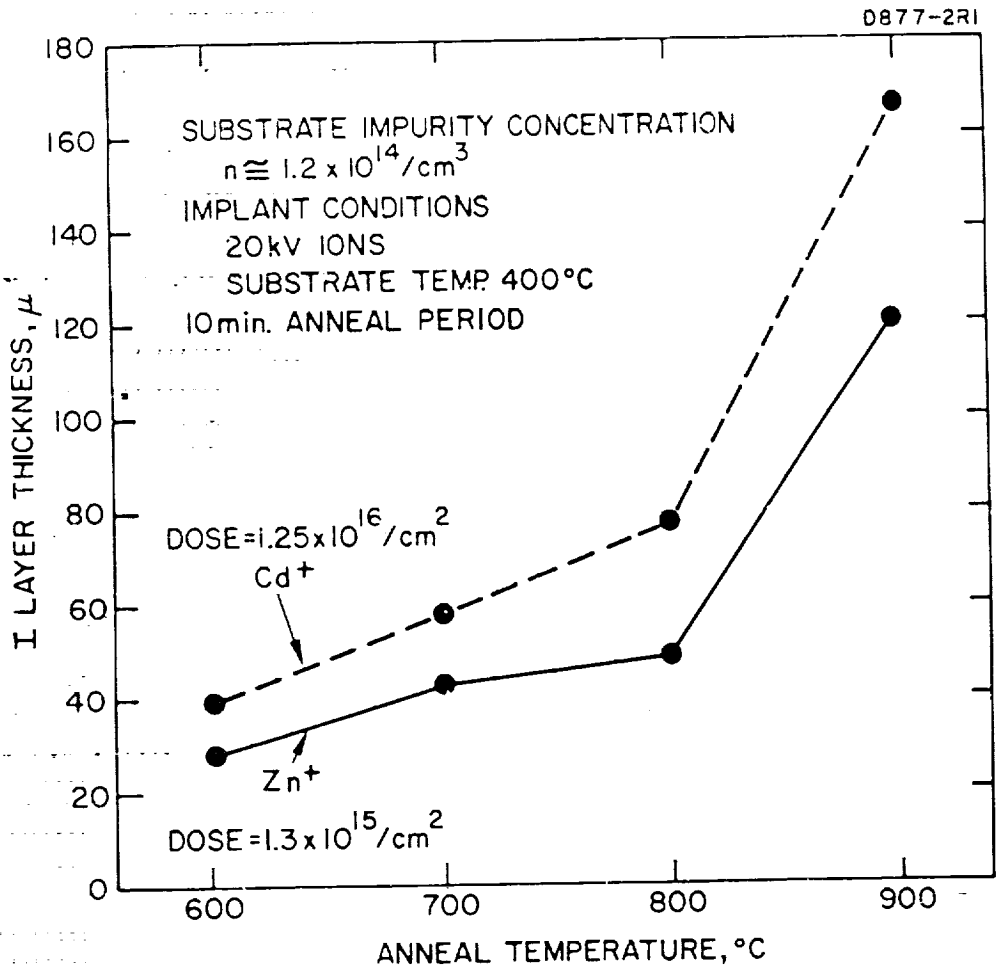


Fig. 13. Dependence of i layer thickness on anneal temperature (for diodes implanted with substrates at 400°C).

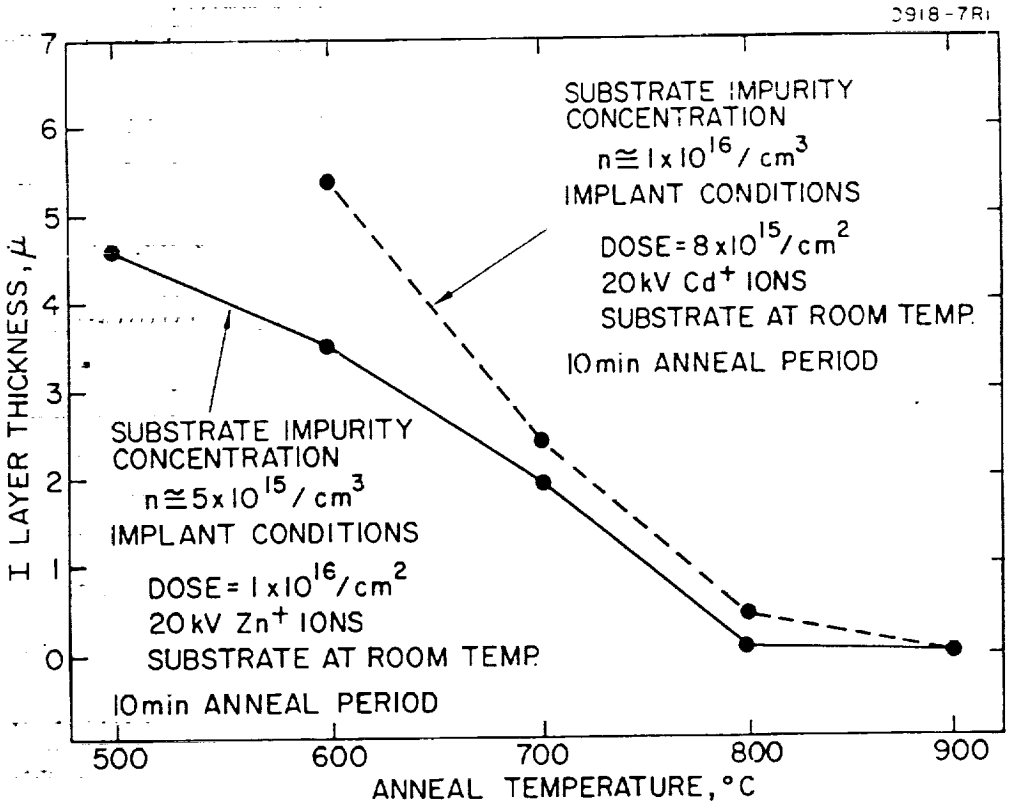


Fig. 14. Dependence of i layer thickness on anneal temperature (for diodes implanted with substrates at 23°C).

in Fig. 15(a), the semi-insulating layer was very thin and in some cases nonexistent. The data of Fig. 15(b) show that even in the case of 400°C implantation, a relatively thin i layer resulted when a very heavily doped substrate material was used. Diodes formed by implanting 20 kV zinc ions into a room temperature substrate (background concentration, $n \approx 1.8 \times 10^{18}/cm^3$) and subsequently annealing at 800 or 900°C for 10 min had the C-V characteristics of an abrupt p-n junction. The reverse breakdown voltage of these diodes was also that which would be theoretically expected (Ref. 4) for an abrupt p-n junction.

The defects responsible for the observed compensation in the i layer diodes are thought to be complexes involving arsenic vacancies and the substrate background dopants (Te or Sn). Compensation involving the implanted p-type dopants zinc and cadmium does not appear to be responsible for the semi-insulating layer because the i layer thickness in many cases far exceeds the projected range of the implanted ions, as well as their diffusion depth for the anneal cycles used. The diffusion depth of implanted zinc and cadmium atoms has been measured using the angle-sectioning method in conjunction with an etchant which stains the p-type layer to permit visual observation of its thickness. The results for zinc implants, which were shown in Fig. 10, indicate a diffusion depth of only 1 μ even after anneal at 900°C for 3 hours. Unlike the semi-insulating layer thickness, the thickness of the p-type layer is essentially independent of substrate background doping concentration. Based on the data of Fig. 10, the calculated diffusion coefficient for ion-implanted zinc at 900°C is on the order of 10^{-13} cm^2/sec, assuming diffusion from a surface layer containing a fixed quantity of atoms. However, this should be considered as only an "average" value since the diffusion coefficient of zinc in GaAs is known to be dependent on the zinc concentration rather than constant (Ref. 3). Angle-section and stain measurement of the depth of 20 kV cadmium-implanted layers has shown that the depth is approximately 3000 Å, and there is negligible change in layer thickness during anneal at temperatures from 600 to 900°C for up to 3 hours. This is to be expected because the diffusion coefficient for cadmium is several orders of magnitude less than that for zinc in GaAs (Refs. 3, 6). While the compensating defects do not involve the implanted ions themselves, the damage resulting from implantation is required for defect generation. This fact was demonstrated by implanting n-type GaAs substrates with 30 keV argon ions, which are not electrically active in GaAs, and subsequently annealing for 1 hour at either 500°C or 600°C. Identical substrates

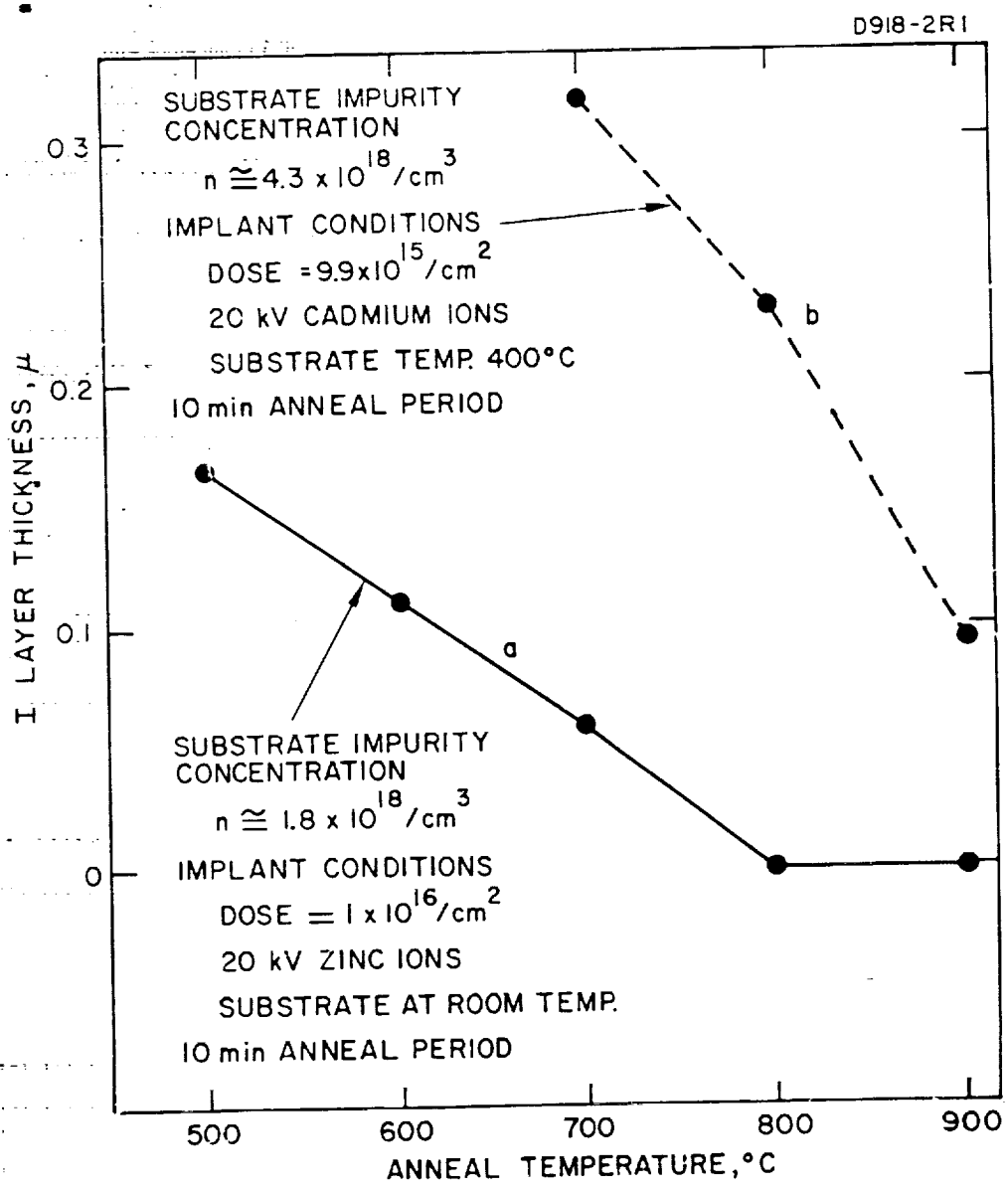


Fig. 15. Dependence of i layer thickness on anneal temperature (diodes implanted into heavily doped substrates).

were subjected to exactly the same heat treatment but were not implanted. Evaporated platinum surface barrier contacts were formed on all of these substrates, and C-V measurements indicated a semi-insulating layer in the implanted substrates, but not in the others. Annealing for 1 hour at 500°C or 600°C is known to be sufficient to produce a high-conductivity layer when electrically active atoms are implanted, indicating that most of the implantation-caused lattice damage has healed. The i layer observed in the argon-implanted substrates after annealing thus appears to result from compensating defect centers such as those present in the zinc- and cadmium-implanted diodes.

The fact that room temperature implantation results in a thinner semi-insulating layer than that formed in 400°C implants after annealing suggests that vacancies generated during implantation may be involved in the compensating defects. Arsenic vacancies rather than gallium vacancies are suspected because the phase diagram of GaAs (Ref. 7) indicates that an arsenic deficient, nonstoichiometric compound will tend to form at the temperatures used for anneal of the i layer diodes. The electroluminescent spectrum of forward-biased zinc-implanted diodes, measured at 77°K, provides additional evidence that arsenic vacancy defect complexes are present. A relatively intense, broad emission band was observed, centered in the range 1.2 to 1.3 eV (see Fig. 16). Increasing the diode anneal temperature in the range 500 to 900°C resulted in a decrease in the intensity of this emission relative to that of the near-bandedge radiation at 1.46 eV, and a shift in peak energy from 1.2 to 1.3 eV. A similar emission band, reported by Kressel, et al. (Ref. 8), has been attributed to an acceptor level approximately 0.23 eV above the valence bandedge, probably as a result of an arsenic vacancy or a complex involving an arsenic vacancy. (However, it should be noted that previous authors (Refs. 9, 10) have observed a similar emission band and attributed it to gallium vacancy-substrate dopant atom complexes.) High resistivity layers in vacuum annealed n-type GaAs have also been attributed to arsenic vacancies or complexes by Pearson and Harris (Ref. 7), who have measured the diffusion coefficient of arsenic vacancies in GaAs to be 10^{-11} cm^2/sec at 600°C, with an activation energy of 1.3 eV. Arsenic vacancy generation during implantation can be limited by implanting ions through a thin film protective coating. Some diodes have been made by implanting 150 keV Zn^{2+} into n-type substrates at 400°C through a 700 to 900 Å thick film of sputtered SiO_2. Following anneal, many of these

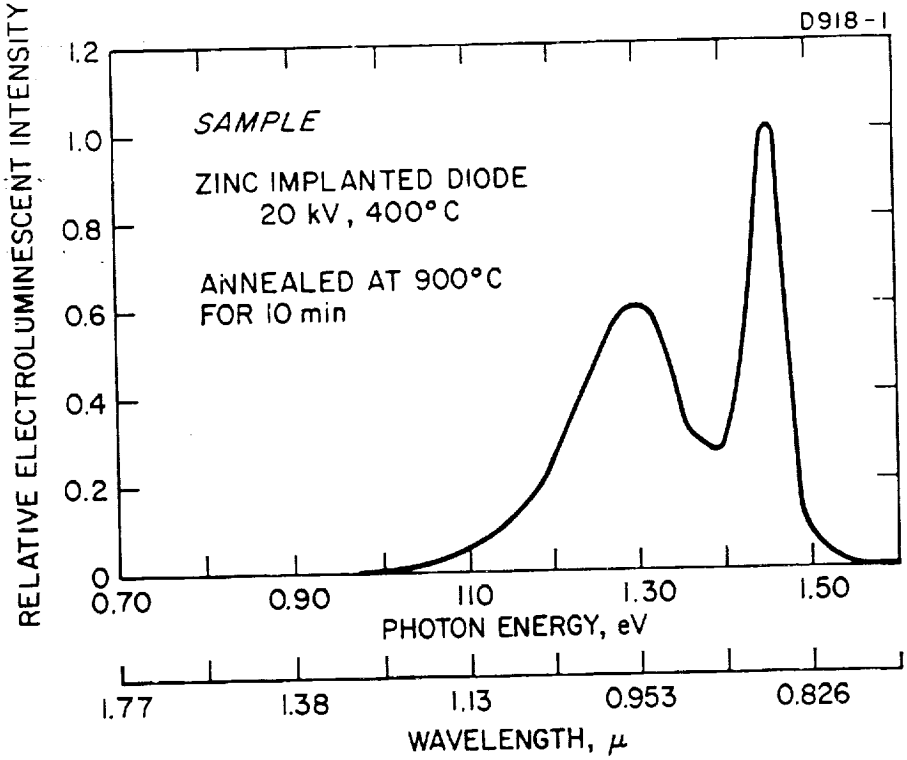


Fig. 16. Electroluminescent spectrum of zinc-implanted GaAs diode.

diodes had abrupt p-n junctions, in marked contrast to diodes implanted at 400°C without the oxide; however, the results of this method were not entirely successful because many other diodes implanted through the oxide had relatively thick i layers. Pinholes observed in the thin oxide may have allowed local escape of arsenic at random points on the substrate. The pinhole problem can be solved by implanting higher energy ions, which would allow the use of thicker, more reliable films. A 300 kV implantation machine is nearing completion at Hughes Research Laboratories, making such experiments feasible.

The compensating defect complexes observed in the zinc and cadmium-implanted diodes do not appear to be strongly dependent on the substrate dopant atom, since both tin and tellurium doped substrates were used and the semi-insulating layer had the same characteristics in both cases. In fact, similar compensation-produced i layers have been observed in n-p diodes made by implanting 85 keV sulfur ions into p-type (zinc doped) GaAs substrates. The vacancy-substrate dopant atom complex presumably produced compensation in these p-type substrates by preventing electrical activity of the zinc acceptors, although it also might have compensated the implanted sulfur donors. Overcompensation, resulting in conversion of an n-type material to p-type, or vice versa, has not been observed.

The conclusion which can be drawn from these results is that the effects of both lattice disorder and nonstoichiometry must be considered when binary compounds are doped by ion implantation. Implantation-caused lattice disorder can be "healed" by annealing at elevated temperature, but steps should be taken during both implantation and anneal to prevent dissociation of the substrate. In ion-implanted substrates it appears that significant dissociation (in terms of vacancy generation) can occur even at temperatures far below the dissociation temperature for the undamaged material.

G. Future Plans

The damage studies and measurements of electrical properties of implanted layers will be continued, with emphasis on higher energy implants (up to 300 keV) at room temperature and 77°K. In some cases implantation through an oxide will be employed to protect the substrate surface.

It is believed that such implantation conditions should minimize arsenic loss during implant and thus result in less defect compensation after annealing has been performed.

The characteristics of ion implanted diodes will be studied as a function of implantation and anneal conditions; the goal of this effort will be to obtain high operating-temperature diodes, efficient light emitters and photodetectors, and possibly IMPATT devices. Efforts also will be made to produce ion-implanted bipolar transistors.

IV. IMPLANTATION STUDIES IN SILICON CARBIDE

Electrically active n-type layers have been created in p-type alpha silicon carbide through ion implantation techniques. Phosphorus, antimony, and nitrogen ions have been implanted at room temperature at ion energies up to 150 keV. Studies of minimal annealing requirements show that diodes with rectification ratios greater than 10^6 at 5.0 V at room temperature can be made using process temperatures no higher than 1200°C while optimum anneal temperatures appear to be 1500 to 1600°C.

A. Nitrogen Implanted into p-Type SiC

The calculated ranges for ions implanted at various energies in an amorphous SiC substrate are seen in Fig. 17. We are deeply indebted to Hans Schiøtt of the University of Aarhus, Aarhus, Denmark, for his computation of the ranges of various ions implanted into amorphous SiC. Such investigation in the case of a mixed crystal is quite lengthy and involves data based essentially on two sublattices. Dr. Schiøtt has compared ranges of ions into a crystal made of equal numbers of $_6C^{12}$ and $_{14}Si^{28}$ atoms and for an equivalent crystal composed of $_{10}Ne^{20}$. The results have been the same in either case, and the equivalent, one-substance model proved to be the most useful in other calculations.

A sample of aluminum-doped α-SiC was implanted with nitrogen at room temperature. This material was supplied by R.B. Campbell of Westinghouse Astronuclear Laboratory, and was doped to a level of $10^{18}/cm^3$. The crystal had been prepared previously by etching in molten sodium peroxide to remove a few mils of material in order to prevent problems which may be caused by possible grown surface layers. The more smoothly etched face has been identified as the silicon face, and was the side implanted. It was then given a two-energy implant with 10^{15} carriers/cm^2 at 84 kV and 10^{15} carriers/cm^2 at 25 kV. As with other implanted samples, the implanted region is dark brown in color and is easily visible. Neglecting possible channeling effects, we expect two concentration peaks at 500 Å and 1500 Å into the SiC. The maximum carrier concentration in each peak should be $\sim 2 \times 10^{20}/cm^3$ and $\sim 10^{20}/cm^3$, respectively. For this situation, the number of implanted ions should equal the number of bulk carriers at 500 Å ± 510 Å and 1500 Å ± 1200 Å (Ref. 11). The effect of overlapping layers should prevent any two-layer or buried junction characteristics. The theoretical distribution curve for these implant conditions is shown in Fig. 18.

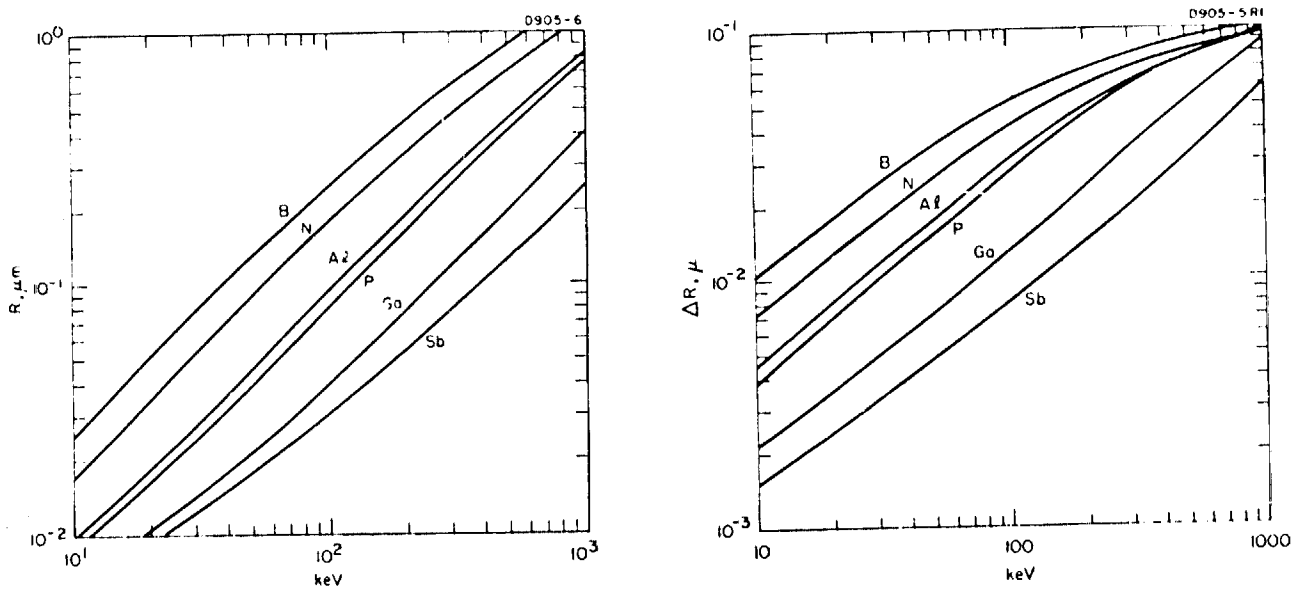


Fig. 17. Range and range-straggling versus energy for ions in amorphous SiC. (Courtesy of H. Schiøtt).

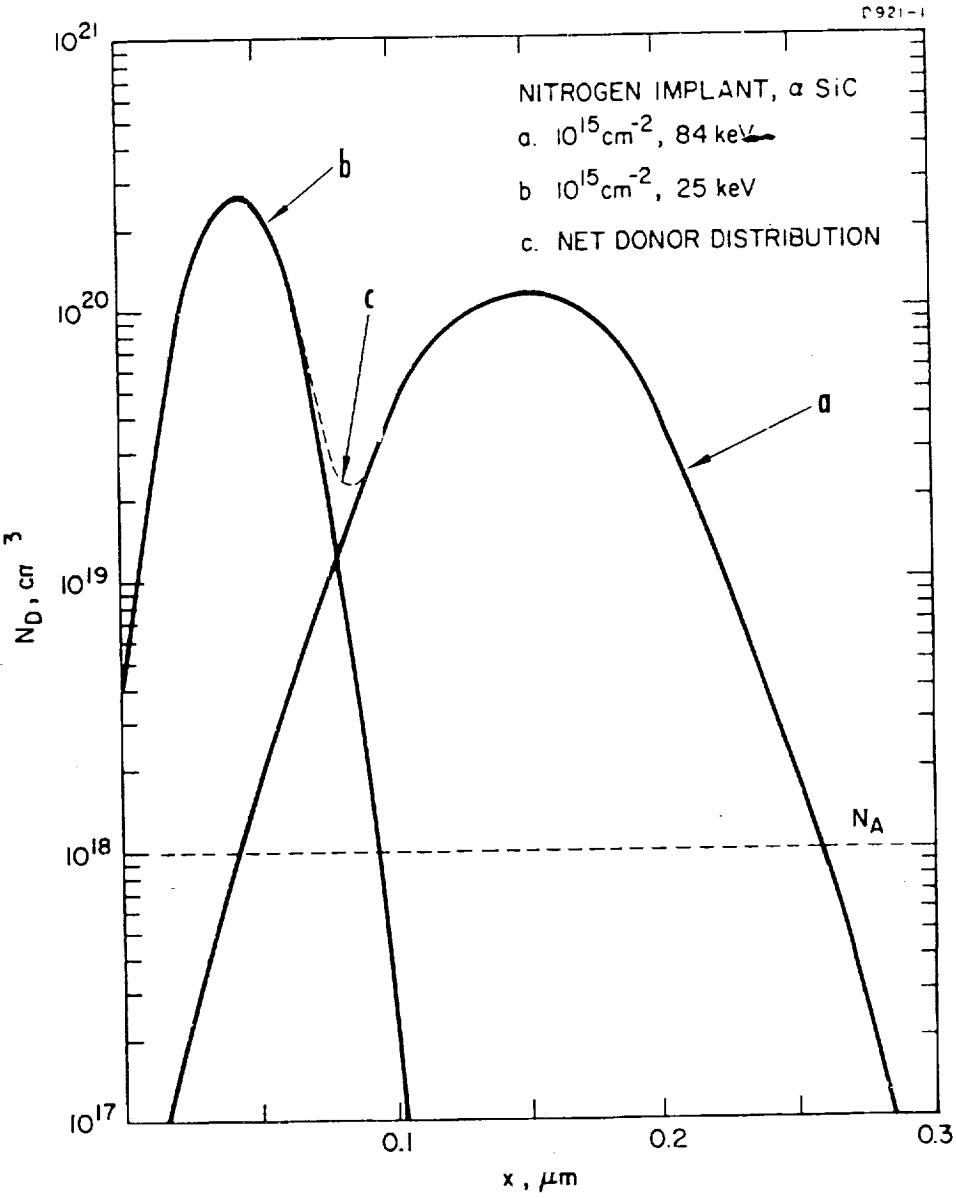


Fig. 18. Theoretical distribution for nitrogen ions in SiC.

As implanted, with no annealing, the surface showed a conductivity and thermal probe response which differed from the original surface of the SiC. Resistivity measurements were nonreproducible, however, and no Hall voltage could be detected. Annealing at 500°C and 750°C resulted in considerable lightening of the brown color and a slight increase in thermal probe response; however, there was no improvement in other electrical measurements.

Annealing the sample at 1000°C in a vacuum of 2×10^{-6} Torr for 2 min increased its response to the thermal probe. Response to ultraviolet light indicated that a p-n junction was present. Soldered indium-silver contacts on the implanted surface permitted Hall measurement with no junction etching required to reduce leakage current. The results of this measurement are shown later in Table I. Junction devices were formed and their characteristics measured in order to investigate the donor-implanted layers. The crystal was masked with wax and a small mesa was etched by anodization (Ref. 12) through the implanted layer into the bulk p-type crystal. Decomposition products must be thoroughly removed from the junction to obtain good device characteristics (see Section IV-F). The mesas were used for capacitance-voltage and current-voltage measurements. Figure 19 shows the V-I characteristics with the possible presence of an ohmic region for reverse bias conditions. The capacitance-voltage relationship shows a drop from 4.12×10^4 pF/cm^2 at zero bias to 2.7×10^4 pF/cm^2 at 30 V reverse bias when measured at 100 kHz. At a constant dc bias of 5 V, capacitance is inversely proportional to frequency rather than maintaining a constant value. This indicates the presence of traps in the junction region (Ref. 5).

A subsequent anneal in vacuum at 1200°C for 2 min produced evidence of a change in sheet resistivity and electron mobility (see Table I). The values of electron mobility listed in Table I are considerably lower than some reported in the literature. However, as a result of charge scattering, a low mobility value is to be expected when the concentration of carriers is high. Electron mobility may also be limited by crystal imperfections which are present following the implantation process. While the state of the art in SiC production is such that it is hazardous to compare data from material from different sources, extrapolation of published data (Ref. 13) indicates that a mobility of 1 cm^2/V-sec is lower than expected if charge scattering is the only mechanism depressing mobility values.

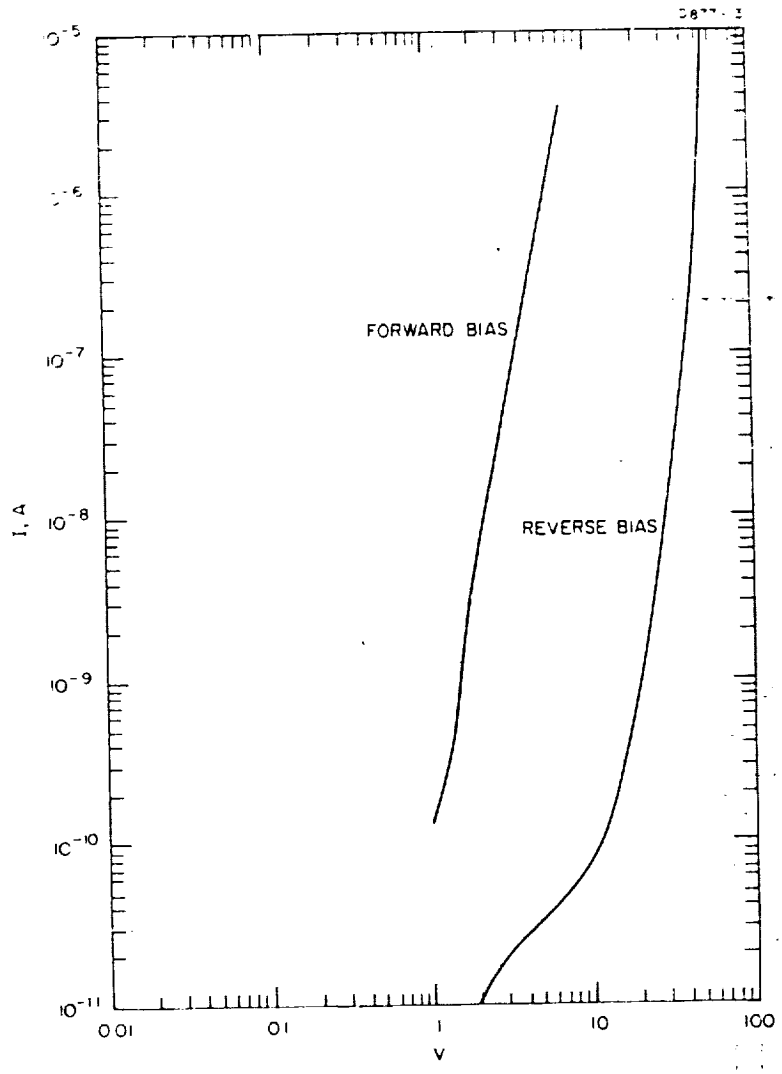


Fig. 19. Current-voltage characteristics of a nitrogen-implanted SiC layer annealed 2 min at 1000°C.

Current-voltage characteristics of a small dot isolated by electroetching contained no indication of an ohmic region. Capacitance as a function of frequency showed much less decrease with increasing frequency than in the previous anneals. The capacitance at 5 V reverse bias is nearly constant at 4.5×10^4 pF/cm^2 from 5 kHz to 500 kHz. Capacitance changes with voltage are shown in Fig. 20; changes occur more rapidly after 1000°C anneal. The above is strong evidence that the defects which cause deep traps in the SiC have annealed out.

An unexpected by-product of the 1200°C anneal was the change in reaction to electrolytic etching. At lower anneal temperatures the products of the electroetch were not entirely soluble, (this situation is described more fully in Section IV-C). Following this last anneal step, the reaction products appeared to be completely soluble, and SiC was removed from etched areas instead of merely being transformed into a nonconductive mass, as was the case previously. This improved etching implies a larger hole current in the n-type layer. The most likely cause for the improved hole current is a decrease in defect centers in the intrinsic regions, or a return to a more ordered crystal form in the donor layer.

In an effort to verify the thickness of the donor region, an angle of 3° was lapped at the edge of the nitrogen-implanted layer. This magnifies the 0.2 μm penetration distance to 3.8 μm, a dimension easily seen by both a light microscope and the scanning electron microscope. However, electroetching of this beveled edge showed none of the expected junction delineation This sample did collect electron bombardment induced (EBI) current efficiently, and allowed examination with the SEM (Refs. 2, 14). At magnifications up to 10,000x, however, no extension of the collecting surface into an angle lapped region could be seen. It would appear that the lapped, but not subsequently annealed, surface is damaged enough to interfere with EBI current collection.

An etched edge of this sample was also examined by the SEM, but no depth was detected in the region collecting the EBI current. Work on other samples has shown that an etched surface will not respond to EBI current examination until it has been subsequently annealed. This anomalous behavior of the p-n junction under chemical and electrical examination has not been satisfactorily explained, but SEM studies after annealing will be continued.

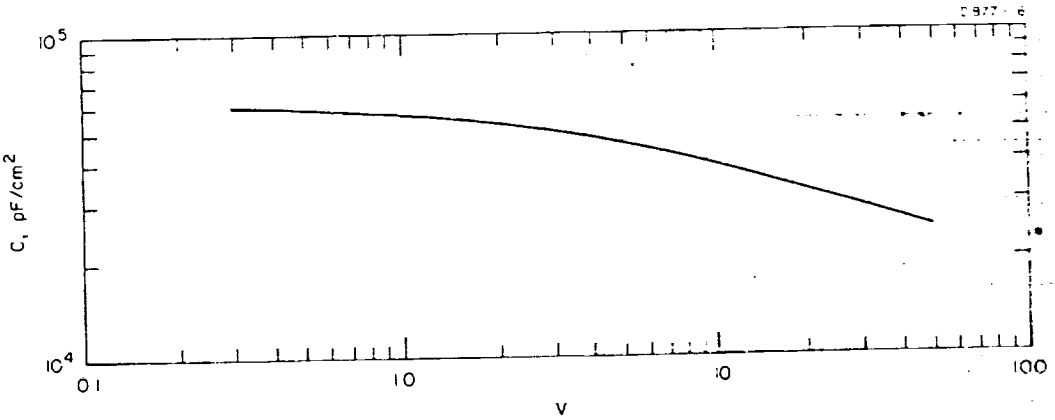


Fig. 20. Capacitance-voltage characteristics of a nitrogen-implanted SiC layer annealed 2 min at 1200°C.

This nitrogen-implanted sample was then annealed at 1400°C for 2 min in a vacuum of 2×10^{-7} Torr. Changes in implanted layer characteristics are summarized in Table I.

Extrapolation of data presented by Kamath (Ref. 13) indicates that the observed mobility of 7 cm^2/V-sec is within a factor of three or four of the electron mobility in SiC grown with a carrier concentration of $10^{20}/cm^3$. This concentration is predicted for our implant conditions by the LSS theory. The sheet carrier concentration of $7 \times 10^{14}/cm^2$ measured for this implanted surface is near that of the total implanted dose ($2 \times 10^{15}/cm^2$).

At this stage of annealing, injection luminescence is observed in the nitrogen-implanted diodes at only 9 mA/cm^2, while a commercial SiC luminescent diode requires 1.1 A/cm^2. The higher current required by the diffused devices is thought to be mostly leakage current, rather than indicating a much less efficient junction.

Figure 21 shows the current-voltage oscilloscope trace of the 1400°C annealed nitrogen-implanted diode. Traces are shown for operation at room temperature and at 300°C. While the forward current has increased as expected, there is little observed change in reverse current out to the breakdown voltage. C-V measurements on these devices indicate that a p-i-n junction similar to that described by Greebe (Ref. 15) exists in the crystal. Figure 22 is a plot of V-I measurements taken at 23°C and 400°C. The forward current characteristic at room temperature exhibits a slight leakage current that has not been removed entirely by the surface cleaning process. Current at both temperatures may be expressed by $I = I_o (\exp (eV/2kT) - 1)$ over a considerable range. A value of I_o may be obtained by extrapolating the curve of exp (eV/2kT) to zero bias. From the data in Fig. 22 and additional measurements at 100°C, 200°C, and 300°C, it is found that I_o is proportional to exp-(1.45 e/kT). The agreement between 1.45 eV and an energy of one-half the bandgap of SiC is significant and suggests that the origin of the current is recombination in the depletion region (Ref. 16). A component of the current above 1 V at 400°C is proportional to exp (eV/kT), which suggests a component due to diffusion current. At higher values of forward current, the I-V characteristic is controlled by a series resistance which can be attributed to the substrate resistivity.

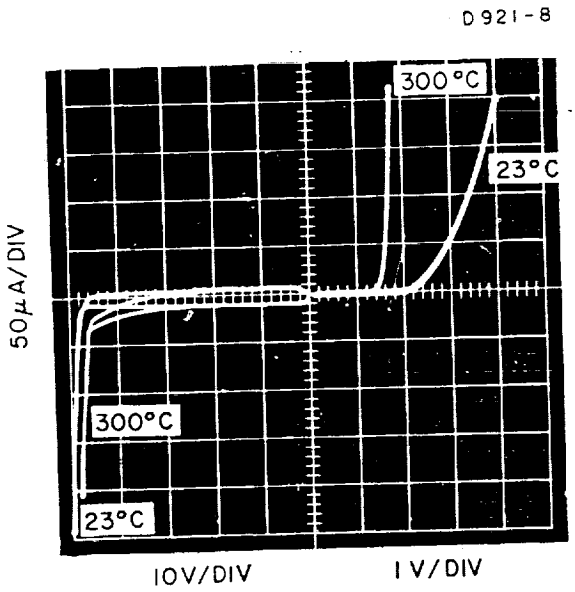


Fig. 21.
Current-voltage trace of nitrogen-implanted SiC diode operated at 23°C and 300°C.

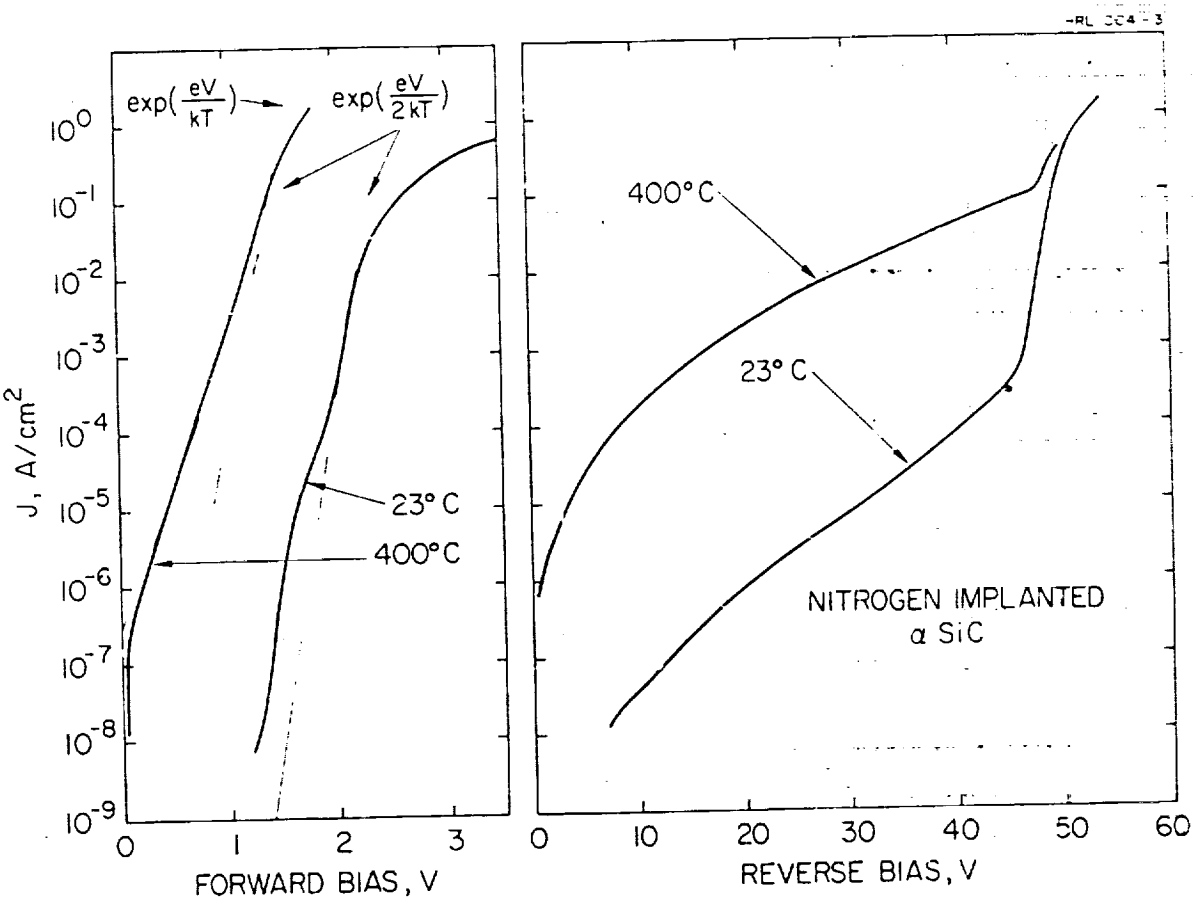


Fig. 22. Log current-voltage plot of nitrogen-implanted SiC diode operated at 23°C and 400°C.

The reverse characteristics of the diodes are of excellent quality and are similar to those found by Brander and Sutton (Ref. 17) on epitaxially grown junctions. The reverse current increases smoothly with applied voltage until an avalanche breakdown is observed at 46 V. Small "blue spots" (Refs. 15, 17, 18) are seen to appear at breakdown; they are located at etch pits which were present in the crystal prior to implantation. Photomultiplication is observed at bias voltages below breakdown with ultraviolet light incident on the junction area.

Electron diffraction examination of the surface after 1400°C annealing showed that the surface had not reverted to its crystalline condition. The low-angle electron diffraction technique can describe only the top 50 Å or so, and this finding is not inconsistent with the observed p-n junction behavior which indicates good crystal structure in the region of the implanted junction, as much as 3000 Å beneath the surface.

Following an anneal in vacuum at 1500°C, electron diffraction detected crystalline structure at the surface. This structure is less well ordered than before implantation, but the amorphous quality of the surface layer has been removed. A concomitant decrease in sheet resistivity of the SiC surface from 1290 Ω/□ to 744 Ω/□ was measured.

Annealing the sample at 1600°C in vacuum served to decrease the sheet resistivity to 198 Ω/□, but the electron diffraction did not indicate any further improvement in the surface structure.

A summary of the Hall measurements as a function of anneal temperatures is shown in Table I.

If N_s is presumed to be $10^{15}/cm^2$ for all anneal stages, the increase in mobility with increasing anneal temperature is a smooth curve represented by the μ^* column of Table I and is plotted in Fig. 23. N_s is derived from the relationship of the Hall voltage, the current, and the magnetic field. A relatively small error in any of these measurements could have caused the observed decrease in N_s at the second and third anneal stages; and the assumption of constant N_s is not unreasonable.

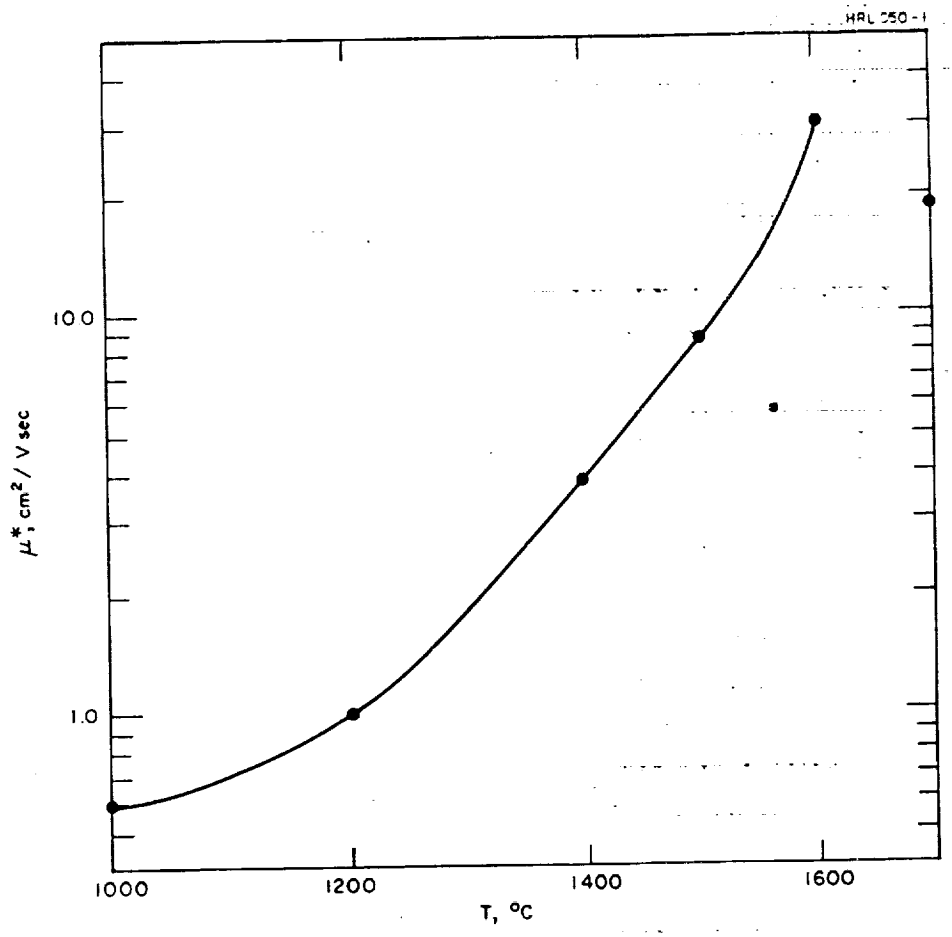


Fig. 23. Carrier mobility versus anneal temperature, nitrogen-implanted SiC.

TABLE I

Results of Hall Measurements of Nitrogen-Implanted Silicon Carbide[a]

Anneal Temperature, °C	V_H/I	N_s, cm^{-2}	σ_s, Ω/□	μ, cm^2/V-sec	μ*
Nonannealed			6×10^6		
1000	0.581	10^{15}	1.06×10^4	0.59	0.588
1200	0.61	9×10^{14}	6.2×10^3	1.0	0.99
1400	0.82	7×10^{14}	1.29×10^3	6.9	4.85
1500	0.549	10^{15}	7.44×10^2	8.4	8.4
1600	0.546	10^{15}	1.97×10^2	31.6	31.6
1700	1.59	3.5×10^{14}	9.55×10^2	18.7	—

[a]All measurements made in magnetic field of 9000 G.

If the carrier concentration in the implanted layer is considered, a mobility of 30 cm^2/V-sec is expected to be the maximum obtainable (Ref. 13). To verify this experimentally, a higher-temperature anneal was used. The sample was annealed in vacuum at 1700°C for two 1 min periods. Surface decomposition resulted in a thin, black, powdery coating (see Section IV-F). The sample was then heated in oxygen to 1000°C for 8 hours to oxidize any free carbon or silicon resulting from the decomposition. There is no way of directly determining the amount of material removed, but the 0.3 μm n-type layer has not all been destroyed. The p-n junction is still present but the injection luminescence is limited by the sheet resistivity and is less bright. Results of Hall measurements are shown in Table I. The drop in mobility is not inconsistent with our previous statement that the annealing of the crystal proceeds outward from the implanted-nonimplanted interface. While the improvement in crystalline order should cause an increase in mobility as shown in Table I, carrier concentration should tend to limit mobility in any given region. For a layer containing the doping profile shown in Fig. 18, two regions of low mobility

would be centered about the areas of maximum concentration, with regions of higher mobility elsewhere. The measured effective mobility of the layer should be some combination of the regional mobilities (Ref. 19). For the distribution shown, if 0.1 μm were removed, only the lower-mobility region would remain, and the effective mobility must drop.

B. Phosphorus Implanted into p-Type SiC

Phosphorus has been used to create p-n junctions in α-SiC. p-type SiC doped to a level of $10^{18}/cm^3$ was used as a substrate, and two room-temperature implants were made with $5 \times 10^{14}/cm^2$ at 145 keV and $1 \times 10^{14}/cm^2$ at 50 keV. This crystal was not etched before implantation, and distinction between the silicon and carbon faces was not made. The calculated doping profile places two regions with peak concentrations of $2.7 \times 10^{19}/cm^3$ and $5.5 \times 10^{19}/cm^3$ at 0.04 μm and 0.12 μm, respectively, with the p-n junctions about 0.18 μm beneath the surface.

Following implant and prior to anneal, the sheet resistivity is measured to be on the order of 2×10^5 Ω/□. This measurement was possible only at currents ≤ 1 μA, and contact noise prevented any Hall measurement. Annealing at 1000°C and 1200°C made no significant change, but Hall measurements were possible after a 2 min anneal at 1400°C. The implanted layer is confirmed to be n-type, with 1.5×10^{14} donors/cm^2, having a mobility of 15 cm^2/V-sec and a sheet resistivity of 2.6×10^3 Ω/□.

C. Antimony-Implanted into p-Type SiC

Singly-ionized antimony was implanted into p-type α-SiC at room temperature. Implantation was carried out on the side of the crystal which was more nearly a smooth, plane surface. This has been presumed to be the silicon face, but x-ray verification was not made. The carrier concentration in the base material was $10^{18}/cm^3$ aluminum atoms. An antimony dose of 10^{15} ions/cm^2 was implanted with a 140 kV Sb beam aligned to within a 1/2° of the major C-axis. The sample was aligned using the proton backscattering technique, described in the appendix. Before anneal the implanted area was easily visible as a dark brown color.

The range of a channeled ion is expected to be considerably greater than that of one which strikes the crystal at a random angle. Some ions which strike the channel will eventually be dechanneled through interaction with lattice atoms, while others will strike the surface atoms. The ions from these sources eventually cause an amorphous region to form, after which channeling ceases. In silicon, a dose of about 10^{14} antimony ions in a channeled direction will cause the amorphous layer to form. Most of the ions then are implanted into the amorphous layer.

If an amorphous range were assumed for the implanted ions (see Fig. 17), most of the implanted ions in a layer would be expected to be centered about a depth of 400 Å in the material. If all were electrically active this would give an average peak carrier concentration of $4 \times 10^{20}/cm^3$ in the implanted layer. This value is obtained when one assumes a gaussian distribution of the implanted ions and uses the data from Fig. 17 as indicated in Gibbons' paper (Ref. 11). Calculation of the distribution of carriers about the peak shows that the concentration will drop by two orders of magnitude at a distance of $3\Delta R_p$ on each side of the peak. This implies that the concentration of the implanted carriers will drop to that of the bulk material at 100 Å and 700 Å inside the material. Based on this estimate, no buried junction is expected on the surface side of the implant distribution.

The implanted crystal was annealed at temperatures up to 1700°C. Anneals below 900°C were performed in a nitrogen atmosphere, but those at higher temperatures were done in vacuum to help prevent oxidation. Electron diffraction examination indicates that complete annealing has not occurred in the temperature range used to date. However, the annealing eliminated all the brown coloration caused by the implantation. The color lightened with each anneal step from 500°C to 1000°C, and was not easily seen after heating to 1000°C. The implant site could still be distinguished visually, but only by observation with transmitted light under moderate magnification. The implanted area is slightly grayer than the untouched crystal.

The electrical characteristics of the implanted layer also changed with annealing stages. After anneal at 500°C for 90 min the current measured by the thermal probe was affected by light from a tungsten lamp as well as a mercury arc lamp with emission lines at 2537 Å, 4358 Å, and 5461 Å. Thermal probing of the implanted layer in the dark gave no detectable current. When the sample was illuminated, the

probes on the antimony-implanted layer responded as with n-type material. When the probes were placed across the boundary between the implanted and nonimplanted areas, the response was similar to that from a p-n junction. Current-voltage measurements of this junction appeared to be limited as a result of very high contact resistance. The sample did not respond to light through a silicon filter. After 1000°C anneal, the light sensitivity was great enough to be detected on the diode current tracer used for V-I measurements, although the V-I measurements themselves were still contact limited. The light response was consistent with that of a p-n junction, with the antimony layer serving as the donor side.

An anneal at 1200°C served to establish a clear p-n junction response. Thermal probing (Ref. 20) across the junction, with and without light, and V-I characteristics of a small anodized-etched mesa verified this.

At annealing stages below 1200°C, the conductivity of the surface was observed to increase; however, the results of resistivity measurements still exhibited such nonlinear characteristics that they could not be correlated. Hall measurements on the layer were also ineffectual. After 1200°C, a small dot was masked with Apiezon W wax and the surrounding SiC was electroetched (Ref. 12). The implanted surface did not "etch" (as etching is customarily described) because the material was not removed, but was merely made to undergo some not-yet-described transformation and color change.

Figure 24 shows the V-I characteristics of this isolated dot using alloyed aluminum-silicon eutectic dots as a bulk contact. The portions of the curves in which $I \propto V$ are suspected to be caused by the electroetched SiC remaining around the diode mesa. The reverse-biased, C-V measurements showed a constant capacitance of 4.7×10^3 pF/cm^2 to 50 V bias when measured with a Boonton 75A-S8 capacitance bridge at 100 kHz test frequency. The capacitance-frequency behavior of the diode at 10 V reverse bias, taken on a Boonton 75C bridge, is shown in Fig. 25(a).

The constant capacitance with increasing reverse bias and the decrease in capacitance with increasing frequency indicate the presence of deep traps and an i region between the implanted region and the bulk material (Ref. 5). This i region can result from bombardment-caused defect centers or vacancies diffused from the radiation-damage layer, or it might possibly be a region originally grown in the material. Grown layers of different resistivity are not unusual in SiC, but further annealing appears to support the assumption of an implant-caused region rather than a grown region, since a grown region should not be affected by annealing.

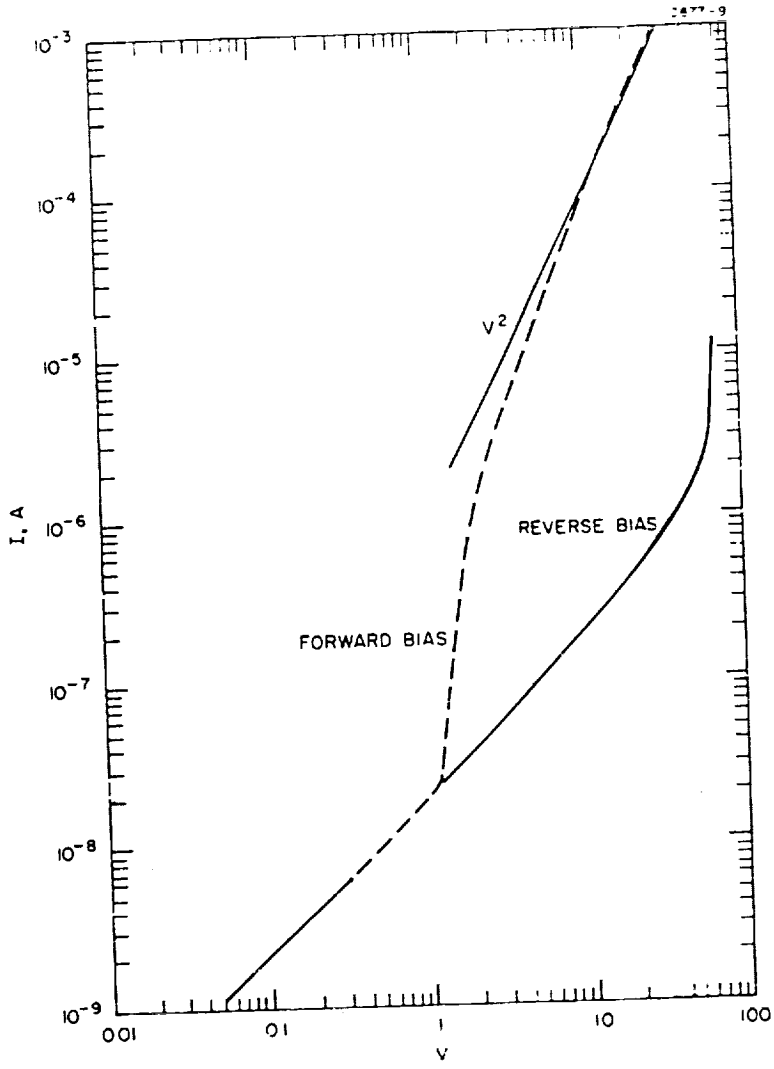


Fig. 24. Current-voltage characteristics of antimony-implanted SiC layer annealed 2 min at 1200°C.

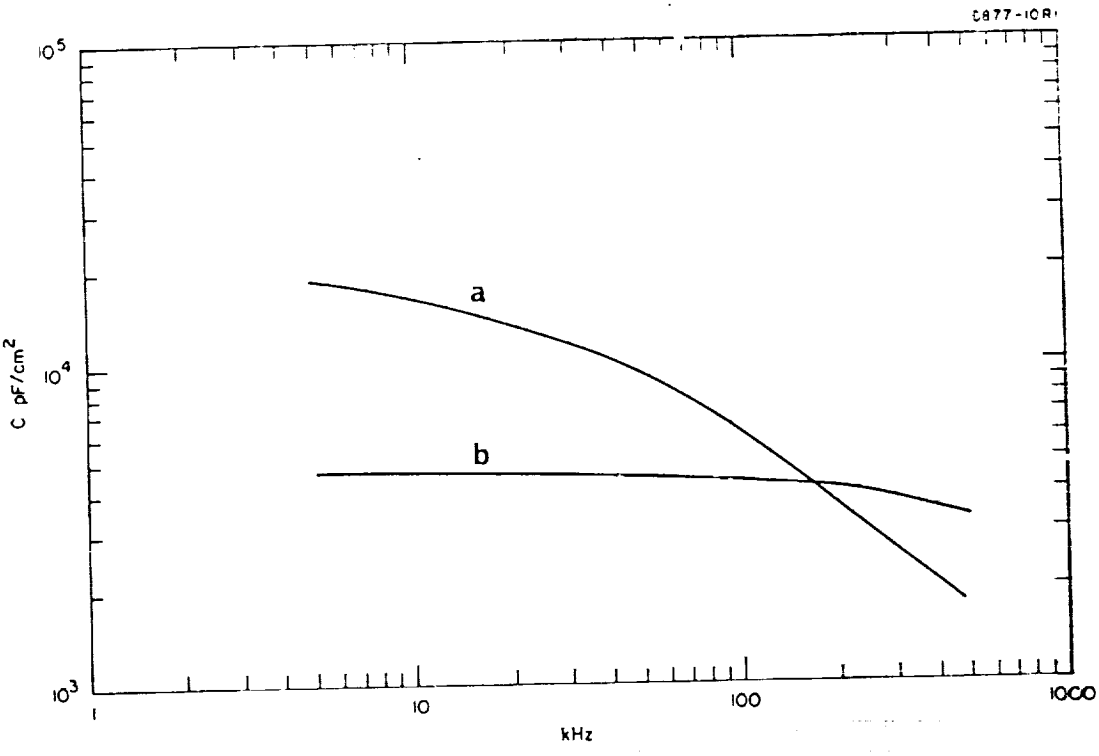


Fig. 25. Capacitance-frequency characteristics of antimony-implanted SiC layer annealed at 1200°C. (a) 2 min anneal. (b) 8-1/2 min anneal.

If the deep trap model is assumed, a minimum i region thickness of 4.6 μm is obtained using the high frequency capacitance value from Fig. 25(a). Using the deep trap model, the decrease in capacitance with increasing frequency can be explained as the inability of the trapping centers to charge and discharge rapidly enough to follow the applied signal at high frequencies. Therefore, the capacitance at high frequencies would be expected to level off at some low value. It is obvious that this condition has not yet occurred, as shown in Fig. 25 at 500 kHz, the highest frequency used in these experiments; thus we can state that the i region thickness is greater than 4.6 μm.

Further annealing for a total of 8-1/2 min at the same temperature caused the V-I characteristics of this dot to degrade severely. In addition, thermal probes changed their response slightly. The sample was then masked with wax except for a small area. The electrolytic etch of the unmasked surface restored the thermal probe characteristics to those obtained before the second anneal at 1200°C. The edge of the etched region indicated that a small amount of material had been removed from the implanted surface. The 1200°C anneal appeared to have changed the surface slightly, and etching removed the changed material.

Electrolytically etching a new mesa in the implanted surface, in the manner described elsewhere in this report, resulted in the removal of material from around the mesa. Soldered indium-silver contacts then were made to both the implanted surface and the bulk material and appeared to serve as excellent ohmic contacts. The I-V characteristics for this device are shown in Fig. 26. Note that the ohmic region observed after the 2 min 1200°C anneal (Fig. 24) does not appear to be present. The effect of illumination from a tungsten lamp on the reverse current is also shown. C-V measurements show that the capacitance per square centimeter has risen to 5.1×10^3 pF at zero bias, but drops to 3.6×10^3 pF at 70 V reverse bias. The variation of capacitance with frequency (Fig. 25(b)) shows less drop in capacitance with increasing frequency than before the anneal. These changes indicate a decrease in the number of trapping centers, which were postulated as the cause of the i region discussed earlier.

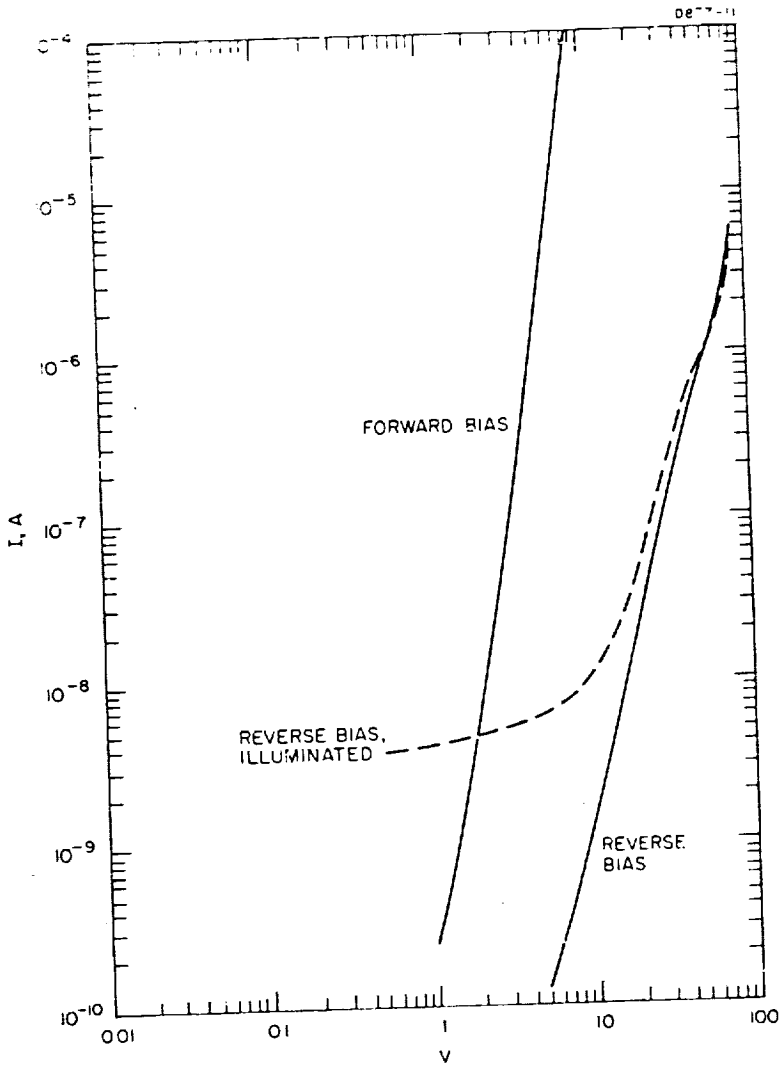


Fig. 26. Current-voltage characteristics of antimony-implanted SiC layer annealed 8-1/2 min at 1200°C.

Hall measurement of a clover-shaped area etched on the surface gave a p-type response. The isolation of the p-n junction around the Hall mesa was not adequate to prevent the bulk carriers from swamping those in the implanted region.

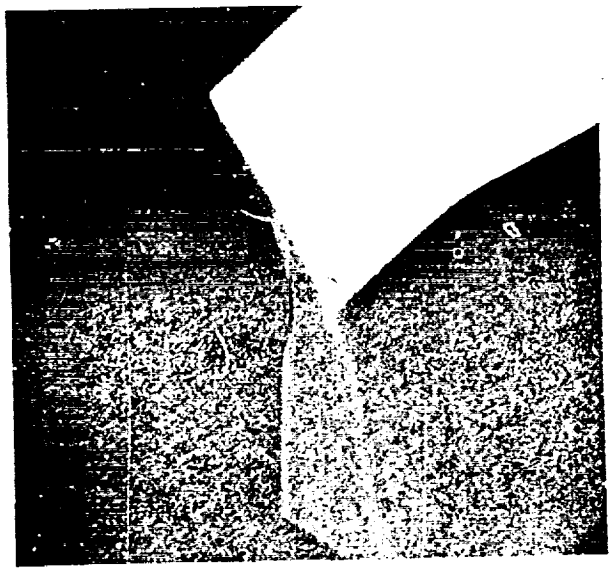
Examination of this antimony-implanted sample using the scanning electron microscope showed that the surface and etched boundaries did not exhibit good collection of electron beam induced current. For most semiconductor surfaces, the electron beam generally induces considerably more current when it is incident on the exposed edge of a p-n region; however, this sample gave no greater signal there than over the rest of the surface. It is assumed that this insensitivity was caused by a combination of the anodizing effect of the etch at the edges and the partially decomposed surface mentioned earlier.

The greater penetration of the implanted ions which is afforded by the channeling process was demonstrated when a small region of the sample responded to the EBI current. This was a region near some small crystals growing out of the surface. The area of enhanced collection was not physically identifiable except through the EBI current examination. Figure 27 shows a portion of this area. Both photographs are at 2000x magnifications. Figure 27(a) shows the surface as "seen" by secondary electron emission, which reveals all surface structure. The white region in this photograph is a very thin film left by some electrolytic etching of the p-type bulk. Figure 27(b) is the EBI current mode and clearly delineates the responsive region. The growth step in the crystal serves as one boundary, but the other boundary is unexplained. The indications are that this area is a crystallite which is not aligned with the large area and hence is not aligned with the implanting ion beam. The interpretation is then that this area has a shallow implanted region which would respond better to EBI current measurement.

To determine the actual implant depth, a 3° angle section was lapped on an edge of this sample. This effectively magnifies the minimum measurable distance to 1.3 μm. This distance is not easily measured optically, but it should be detectable and is well within the range of the SEM. However, the antimony-implanted surface, annealed to only 1200°C at the time of the first study, served as a poor collector of electron beam induced current and could not be examined then by the SEM.

SECONDARY EMISSION (2000X)

(a)



EBI CURRENT (2000X)

(b)

Fig. 27.
SEM micrograph of responsive area in antimony-implanted SiC.

Since the electrolytic etching of SiC is effective only on p-type material, junction delineation was expected when the angle-lapped portion was etched. Preferential etching was present, but there was no "lip" on the n-region to suggest penetration into the bulk material. The SiC etched to the edge of the lapped region. It is possible that the bias used in the etching process caused sufficient injection to "wash out" the resistance of the junction area to the etching process. Low-bias etches were attempted, but they failed because the work-damaged lapped surface was unexpectedly resistant to the etch.

After a 1400°C anneal, the lapped surface etched at a low bias, but still there was no indication of any depth to the junction. Re-examination by the SEM using a wide range of beam voltages and angles of incidence has developed considerable detail in the structure of the sample, as seen in Figs. 28 and 29.*

Figure 28 shows a portion of the antimony-implanted surface after it has been electrolytically etched and annealed at 1400°C. The beam energy of the SEM is 20 kV. Figure 28(a) shows the surface by secondary electron emission. Various smaller holes in the donor layer are denoted only by the dark shadows of small spaces that were either etched into the SiC or originally in the p-type bulk beneath the surface. The antimony-implanted layer strongly resisted the etch. A beam voltage of 5 kV showed no evidence of these spots because it did not penetrate sufficiently. The larger holes have lost the donor layer cover because of its fracture, although traces of it can still be seen at the edges.

Figure 28(b) shows the same area as it responds to EBI current. An explanation of the "ringed" response in Fig. 28(b) is suggested in the information contained in Fig. 29(b). Figure 29 is a SEM micrograph of the side of an etched pit in the SiC. Figure 29(a) shows the secondary electron emission, and Fig. 29(b) the EBI current. Figure 29(b) shows considerable laminar structure to appreciable

*We are indeb ed to E. Wolf for his work with the scanning electron microscope in obtaining these pictures.

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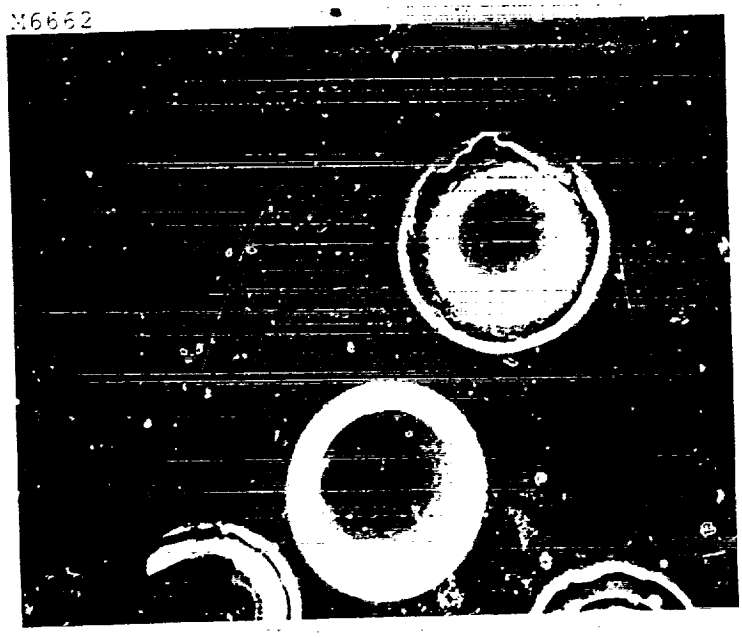
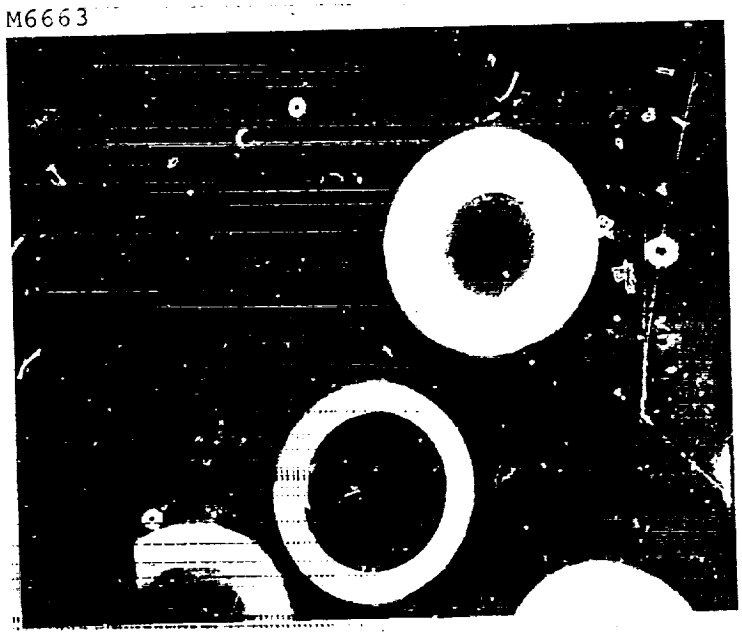


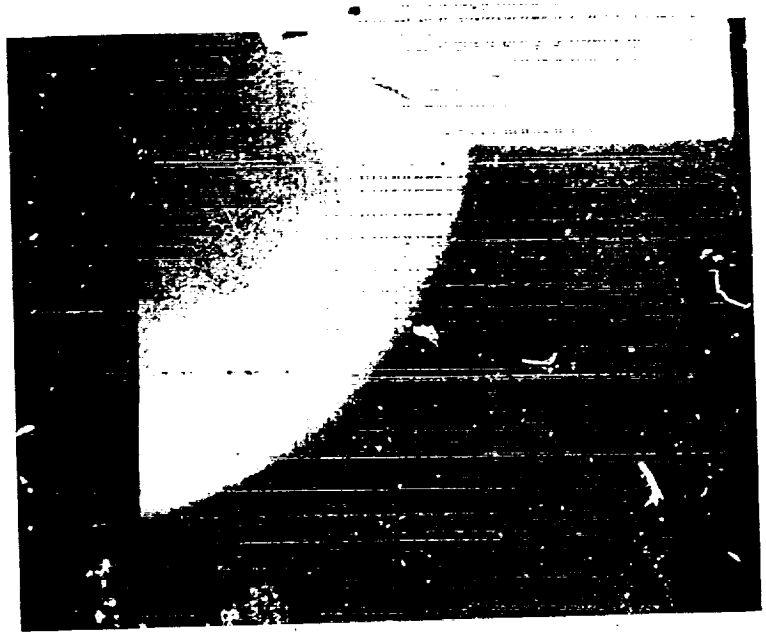
(a) Secondary emission (1100x)

M6663

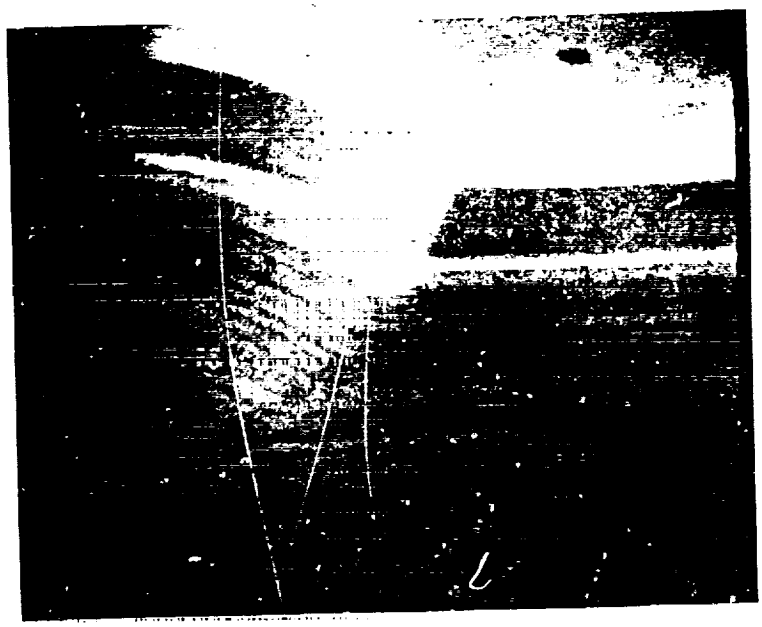


(b) EBI current display (1100x)

Figure [illegible] pinholes in anodized layer in Al.



(a) Secondary electron emission mode



(b) Electron bombardment induced current mode

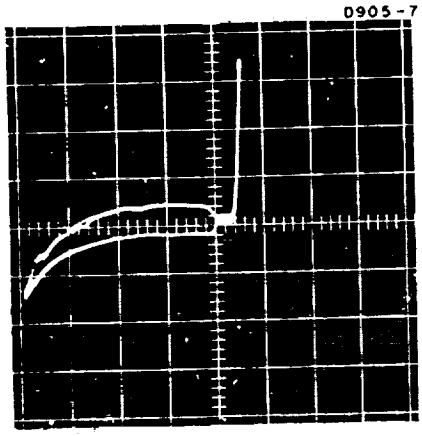
Fig. 29. SEM display of etched wall of antimony-implanted sample.

depths, about thirty distinct layers in the first 15 μm of depth. The rings in Fig. 28(b) appear to result from holes of differing depths. Some of the grown layers in the crystal respond to EBI current much more strongly than does the implanted region. This is thought to result from low lifetime and mobility values in the heavily-implanted layer, but further study will be required to confirm this. The topmost layer shown in Fig. 29 does not have smooth, etched edges but shows distinct conchoidal fracture lines. This appears to be the implanted n-type region which did not etch, but which broke away from the crystal when the supporting bulk was removed. The thickness of this n-type layer is approximately 1 μm. It is not understood why a layer of this thickness was not observed in the angle sectioning measurement. The laminar structure beneath the surface has all etched smoothly and appears to contain no n-type layers or layers of greatly differing resistivity. The individual layers in the crystal appear to be grown regions and are of no assistance in understanding the physics of ion implantation. However, there is no evidence that they unduly complicate the junction effect. In future samples they will be eliminated whenever possible by the use of proper surface preparation.

The V-I characteristics of an etched mesa are similar to those obtained after lower temperature anneals. Figure 30 shows a V-I characteristic after 1400°C anneal. When about 5 mA current is passed in the forward direction, this mesa provides a yellow glow; under reverse bias at the same current, a greenish glow results.

After this sample was annealed at 1600°C in vacuum for 2 min, some surface decomposition had taken place; i.e., all surfaces of the sample showed an increase in conductivity. All etched mesas which were previously electrically isolated were effectively shorted to the bulk, and re-etching was necessary. After re-etching, the V-I characteristics were much the same as before the higher temperature anneal, but the forward resistance of the diode had decreased. Measurements of the diode I-V characteristics at 23° and 100°C reveal little difference in the behavior of the device at the two temperatures.

Sheet resistivity measurements on the implanted layer indicate that the sheet resistivity had dropped to 12 kΩ/□. Hall voltages could not be observed, even though the Hall



x = 5 V/cm
y = 10 μA/cm

Fig. 30.
Current-voltage trace of antimony-implanted SiC diode.

equipment was modified in an effort to increase the sensitivity of the measurement. Values of the Hall coefficient are necessary to determine the sheet concentration N_s and the Hall mobility μ_H. These parameters are particularly important for the analysis of the antimony-implanted layers because this impurity has never (to our knowledge) been introduced and studied as a dopant in SiC.

In an effort to obtain Hall measurements, the sample was annealed at 1700°C in vacuum for 2 min. This heat treatment resulted in only a slightly decomposed layer; however, Hall measurements were still not possible, apparently because of the high sheet resistivity and the difficulty of making low-noise contacts to the sample.

V-I measurements of a diode etched into the Sb-implanted surface after the 1700°C anneal show that the reverse breakdown characteristic is controlled by a large number of "blue spots" (Refs. 15, 17, 18) or avalanche breakdown regions. Injection luminescence is obtained under forward bias, but the surface sheet resistivity limits the luminescence to the immediate vicinity of the electrical probe contact.

D. Acceptor Species Implants

1. Aluminum implanted into n-type SiC. — The efforts to verify acceptor action of ion-implanted aluminum have continued, using β-SiC obtained from Stanford Research Institute which was reported to have residual nitrogen doping to a level of $5 \times 10^{17}/cm^3$. The crystals have flat surfaces, a result of the growth process. One face was implanted with antimony in the spark-gap machine at 500°C to insure ohmic contact to the bulk (Ref. 14).

Aluminum ions prepared by a surface ionization source were implanted into the opposite face at 25 kV for a total dose of 10^{15} ion/cm^2. Distinction between the silicon and carbon faces was not obtained. Work with silicon has shown that at a given anneal temperature the percentage of electrically active carriers is greater for implantation at room temperature than for implantation at higher temperatures. Therefore, the aluminum was implanted at room temperature.

In order that the implanted layer on the small crystal might be examined without heating or alloying steps, gold dots were evaporated on the implanted and nonimplanted surfaces, and C-V and I-V measurements were made of the surface barriers in an attempt to establish the effect of the aluminum implant on the SiC. It was observed that the C-V curves changed with time for any gold dot investigated, possibly as a result of a change in the surface states of the material. There was no evidence that the dots served as a contact to a p-type layer. While the electrical characteristics of the surface barriers on both areas changed, those on the nonimplanted surface showed significantly more change. However, meaningful interpretation of these changes is not possible at present. This sample was examined after implantation, after 850°C anneal, and after 1000°C anneal. The measurements were all self-consistent, but none of them gave any positive indication of a p-type layer in the aluminum implanted region.

Thermal probe measurements after the 1000°C anneal indicated only that the aluminum implant region was less n-type than the nonimplanted region. There was no indication of a junction photovoltage in response to ultraviolet light. Higher temperature anneal studies are required on these implants.

Aluminum has been implanted into the silicon face of a piece of nitrogen-doped α-SiC with about 3×10^{18} carriers/cm^3. Doses of $10^{15}/cm^2$ at 90 keV and $10^{15}/cm^2$ at 40 keV were implanted. Assuming that predictions based on an amorphous substrate can be applied, the average peak concentration is expected to be 2×10^{20} with a junction at 0.16 μm beneath the surface. The SiC was cleaned thoroughly with acid prior to implantation, but no mechanical polishing or high-temperature etches were performed to remove the high-resistivity n-type layer which may exist in this type of material.

The implanted region was considerably darker than nonimplanted parts. Angle sectioning without annealing showed that the brown stain did not penetrate detectably into the crystal. Thermal probing was inconclusive. Annealing the sample at 1000, 1400, and 1600°C for 2 min periods did not significantly alter the electrical behavior of the implanted layer. No response to thermal probing was observed, nor were any signs of junction behavior discovered by either

I-V measurements through the layer or by photoresponse. Annealing in vacuum at higher temperature was not attempted because the SiC decomposes.

2. Boron implanted into n-type SiC. — A piece of n-type α-SiC doped with 1 to 3 x 10^{18} nitrogen atoms/cm^3 was implanted with boron into the Si face at room temperature. A double implant was made with $10^{15}/cm^2$ at 80 keV and $10^{14}/cm^2$ at 20 keV. This should give two overlapping regions of ion concentration extending almost 0.3 μm into the crystal. The peak carrier concentration in the regions is predicted to be 3 x $10^{19}/cm^3$ for the 20 keV ions and 9 x $10^{19}/cm^3$ for the 80 keV ions. These figures are based on the assumption of an amorphous substrate, and may be modified by the crystallinity of the sample.

The crystal surface was acid cleaned prior to implantation, but no attempt was made to remove any surface layers. After implantation, but prior to anneal, the thermal probe showed no definitive response, and gold point contacts on the implanted surface showed characteristics of back-to-back surface barriers.

Annealing the sample at 1000°C for 2 min in a vacuum of 10^{-7} Torr made no detectable change in the implanted layer. Annealing the sample at 1400°C for 2 min in a vacuum 10^{-7} Torr changed the measured characteristics of the implanted layer. Electrical probing showed a nonlinear I-V behavior, indicating that a p-n junction existed across the implanted-nonimplanted interface. Ultraviolet light excited a photocurrent of 10 pA with a polarity which supports the existence of the expected p-n junction. A linear resistance of 67 kΩ occurred between gold points 0.25 mm apart on the implanted surface. By contrast, the same arrangement on the nonimplanted side exhibits only 910 Ω.

Soldered indium silver contacts were applied to the periphery of the implanted layer and exhibited little noise during Hall measurement. The Hall effect and sheet resistivity measurements were indicative of the bulk material and not of the implanted layer. This is to be expected when the p-n junction does not sufficiently isolate the implanted layer from the bulk, as was the case for this sample.

The sample was then annealed at 1800°C for 2 min at 10^{-7} Torr. Considerable decomposition of the SiC surface was observed, and the sample had a black coating on it when it was removed from the furnace. This coating was loose and could be scraped off easily; it was removed by heating in air

to 600°C. After this treatment, there were no indications of an implanted layer. Extrapolation of the data given by Shaffer (Ref. 21) indicates that as much as 0.8 μm of the crystal surface may have been lost at this temperature and pressure. This crystal was heated at 1000°C in dry oxygen to oxidize and clean the distressed surface. Boron was then again implanted into the silicon surface of this sample at room temperature, as described above. The implanted layer did not respond as p-type to the hot probe, either before or after the sample was annealed in vacuum at 1600°C for 2 min. This is to be expected, since boron in SiC is a rather deep level acceptor with activation energies of about 0.4, 0.5, and 0.6 eV (Ref. 22).

An area of the surface of the implant was masked and the surface was electrolytically etched to form a mesa structure. Current-voltage measurements on this device revealed the presence of a p-n junction with a soft breakdown in the reverse bias direction. The rectification characteristics were proper for the boron layer behaving as p-type. However, these characteristics were not dependable and reproducible. It is possible that the rectification resulted from surface conditions rather than an implanted layer. Hall measurements and photovoltage measurements have not confirmed the existence of a p-type region.

We have attempted to make p-type α-SiC by implanting aluminum, boron, and gallium, with no positive success to date. Kal'nin, et al. (Ref. 23), and Maslakovets, et al. (Ref. 24), have reported that beryllium in SiC forms deep acceptor levels and is an activator for red luminescence. A source for the spark-gap machine was fabricated using sheet beryllium contacts and a carbon vibrator to form the arc. A sample of n-type, α-SiC of 10^{18} carriers/cm^3 was then given a room temperature implant at 5 kV. The dose delivered by this machine is undetermined, but the darkening of the substrate was considerably less than that caused by the antimony implant discussed earlier. The calculated range of beryllium in SiC is 200 Å, with a range straggling of 76 Å for the ion energy used in an amorphous substrate.

With reflected light, the implanted surface had a slight metallic color, and lengthy soaking in aqua regia did not change this. Anneal in vacuum at 800°C removed this metallic luster under reflected light, but transmitted light still clearly showed the implanted region.

Thermal probing before and after the anneal did not clearly indicate a conductivity type; perhaps even less signal was obtained after the anneal. Electrical probing in either case showed point contact rectification.

However, a vacuum anneal at 1000°C changed the surface which had been implanted with beryllium to reduce the barrier height to point contacts. The V-I trace between two points on the implanted surface showed ohmic conduction at the origin, while points on the nonimplanted areas showed rectification. The thermal probe gave distinct but weak p-type responses at some small areas of the implanted region. There were no other indications of a p-n junction in the material, however.

Another anneal in vacuum, at 1200°C, lightened the implanted region so that it could not be seen in transmitted light. The thermal probe revealed a weak but reproducible n-type on the implanted surface, while the nonimplanted region gave no type indication. Probes still made ohmic contact to the implanted region but not to the rest of the sample, and the resistance between probes fell to about half the resistance seen after the 1000°C anneal. There was no luminescence observed for the condition of forward bias of a junction. Solder dots made satisfactory contacts to permit Hall measurements, but no Hall voltage was detected for the most sensitive condition.

The net result of the various acceptor-species implants has been the creation of high resistivity regions rather than p-type regions. We have not yet explained the failure of elements to act as acceptors when implanted into the crystal, when these same elements are known to act as acceptors in silicon carbide when assimilated into the crystal during growth or diffusion.

E. Equipment and Methods

The implants discussed in this report were performed in implantation systems built by Hughes Research Laboratories, with one of the systems designed for ion channeling in

crystals. The channeling system and alignment techniques are discussed in the appendix. (Silicon is the material used in this appendix to describe the alignment technique used for SiC.*)

After the impurities are implanted into the SiC pieces, it is necessary to make the ions electrically active. Work with implanted silicon (Ref. 25) has shown that, for a given implanted dose, more electrical carriers are available after low temperature implant and high temperature anneal than with a straightforward high temperature implant.

The samples described in this study have been annealed in a nitrogen atmosphere at temperatures up to, and including, 1000°C, and in vacuum from 800°C to 1700°C. Ervin (Ref. 26) has shown that for the annealing times used here, SiC has negligible oxidation in oxygen below 1000°C and in a vacuum of 10^{-5} Torr or better at temperatures up to 1600°C. The temperature of the samples in the vacuum furnace has been measured using optical pyrometers. No allowances have been made for the variation in sample size or possible emissivity changes, and the actual sample temperatures may have been as much as 100°C higher than those recorded.

In order to study p-n junction I-V characteristics, the SiC has been electrolytically mesa-etched (Ref. 12). This method is effective only on p-type SiC or on thin layers of n-type material where a hole current must be maintained by injection. While this is not an optimum process, it has been adequate for sufficiently well-annealed material.

Electrical contacts to both the bulk SiC and to implanted layers have been made with soldered indium-silver. Alloyed dots of aluminum-silicon eutectic have been used as contacts to the p-type bulk; however, when only reverse-biased junction characteristics were being studied, these alloys were not considered worth the added heat cycle required to reapply contacts after each annealing step. The electrical measurements on the implanted layers have been made at temperatures from room temperature to 400°C. When Al-Si alloy was not used for contacts, simple pressure contacts were used at the higher temperatures; these consisted of a gold probe on the implanted region and a carbon plate on the bulk.

*We wish to thank Dr. R. Hart for this description and for performing the aligned implants.

F. Chemical Treatments

In all of our implantation work, activation of the implanted carriers has required annealing of the damaged crystal. Some temperatures which appear to be required for SiC are sufficient to cause the surfaces of the crystal to undergo changes.

Ervin (Ref. 26) has reported oxidation of SiC in air at temperatures as low as 900°C, with a resultant oxide coating on the crystal. He has also reported that heating in vacua with pressures as low as 10^{-5} Torr results in the formation of volatile oxides and etching of the crystal. Vacuum heating above 1400°C was sufficient to cause reaction with the residual gas in the chamber if the pressure was as high as 10^{-3} Torr; 1400°C is within the temperature range required for adequate annealing of the implanted SiC.

To protect the SiC surface from exposure to the residual gases, the application of SiO_2 and/or Al_2O_3 films has been considered. The temperatures required have not seemed conducive to the use of SiO_2, and Ervin reported that a glassy coating (in his experiments, soda glasses were used) did not slow the oxidation rate; thus we have not experimented with SiO_2.

Imai (Ref. 27) has reported making aluminum-doped tunnel diodes in SiC using an Al_2O_3 source. Because of the limited SiC supply on hand, we will not attempt to protect an SiC surface with Al_2O_3 until other methods have proved ineffective.

A procedure used successfully in the heat treatment of GaAs (Ref. 1) and other volatile crystals has been tried for SiC. In the case of a volatile crystal, it has been shown that the restricted volume maintains an adequate overpressure to prevent boil-off of the compound. SiC is not considered a volatile crystal, and its decomposition mechanism is different. Two crystals were heated to 1700°C in a face-to-face situation, one on top of the other, in a vacuum of 5×10^{-6} Torr; it was anticipated that the restricted flow of residual gas in the confined space between the crystals would prevent the formation of volatile oxides. The top SiC crystal on the heater strip (which was at a slightly lower temperature) collected some small spheres on its surface, and the bottom piece showed evidence of decomposition. The small spheres dissolved in a hydrofluoric acid-based etch and were apparently silicon or silicon dioxide. Obviously the

face-to-face process did not work in this case, although it is possible that some protection could be obtained if the faces were polished and the surfaces mated closely together.

An alternative to vacuum processing is the use of an inert atmosphere. This should prevent such rapid oxidation of the surface by dilution, if by no other method. Harris et al. (Ref. 28), has shown that SiC annealed in an inert atmosphere is very sensitive to trace gases adsorbed on the furnace parts. This observation, coupled with inspection of the low partial pressure of oxygen shown to result in SiC decomposition, indicates that there would be little advantage to using inert gas as a high temperature annealing atmosphere.

Another method of protecting the implanted surface is to bury the implanted layer sufficiently deeply in the SiC that the required annealing will remove enough SiC to expose the implant. This situation is not flexible because it would prevent proper measurement of the implant during a series of anneal temperatures; however, it would appear to be a workable procedure. In this process it would be essential that the decomposed surface not be a degenerate, conductive surface which would short out the implanted characteristics. If this occurred, controlled etching would be required; this is feasible, but it has its own set of difficulties.

To determine a material loss rate, a series of crystals were weighed, heated to 1700°C for 2 to 4 min at 5×10^{-6} Torr, and reweighed to inspect for weight loss. The balance used was the Cahn model M-10 electrobalance with 1 μg sensitivity. This sensitivity was insufficient to detect any weight loss for the examined crystals, presumably since the surface-volume ratio was quite small for the available crystals.

Observations made during the experiments are not reassuring. One of the heated crystals developed a distinct carbon coating which can be removed only by mechanical means or by burning in an oxygen-filled furnace. Another crystal of the same batch, processed in the same way, showed no such soft coating, although it did darken slightly. Other crystals showed neither of these conditions. No clear pattern was discernible in these results.

A method of maintaining a given surface on a crystal, which is frequently used by crystal growers and those engaged in gaseous diffusion processes, seems inapplicable here. This process requires the use of excess amounts of

the volatile constituents and controlling chamber temperature gradients in order to create thermal equilibrium over the crystal being treated. This can curtail the SiC decomposition and protect a buried implanted layer. However, because thermal equilibrium actually involves the exchange of atoms between the crystal and atmosphere, it is questionable whether an implanted layer on the surface could be maintained in such a situation.

While surface decomposition has been detected at temperatures as low as 1400°C, the rate of decomposition is such that there has been negligible effect on the implanted layer at temperatures below 1700°C. Although the surface charges are slight, they have affected the p-n junction measurements. The decomposed layers crossing a p-n junction have served as shunt resistors across the junction. To remove this shunting resistance, and to form a limited-area device for study, electrolytic etching has been used exclusively. This procedure is described thoroughly in the literature (Ref. 12), and only an observation will be noted here.

The response of an ion-implanted surface to electrolytic etching appears to vary with the degree of annealing. It also has been observed to be affected by damage contained in a lapped surface; thus it is assumed to result from implant damage. For surfaces with considerable residual damage, electroetching may not remove SiC, but it will alter its form. The "etched" SiC becomes porous and may be soft enough to scrape with metal tools, but it is not soluble in acids and remains on the crystal. This porous material has fairly high resistivity and shunts the p-n junction characteristics in order to impose an ohmic characteristic (see Fig. 24). Heating this porous material, as in a higher temperature anneal, will allow it to be etched away. After an undetermined degree of crystallinity has been recovered, the electroetch forms soluble products which are removed entirely, and there is no interference with the junction measurements.

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APPENDIX

A. Ion Channeling Research System

For the investigation of ion channeling, a system was designed and built to meet the following requirements:

1. Ion source capable of producing any ion of column III or column V of the periodic table
2. Monoenergetic ions with energy variable up to 160 keV
3. Mass-separated beam
4. Beam divergence less than 0.1^{o}
5. Alignment of the appropriate crystallographic axis of the target crystal with the beam to less than 0.1^{o}.

The completed system is shown in Figs. A-1 and A-2.

The ion source is a Nielsen type (Danfysik) electron bombardment source. A 40-mil tungsten filament is utilized both for electron emission and as an internal heater. The filament power is sufficiently high (400 W) to heat the discharge chamber to 1000^{o}C. The hot discharge chamber prevents recondensation of the charge material which is sublimed in a separate oven crucible assembly adjacent to the chamber. Gaseous charge materials are fed directly into the discharge chamber through a variable leak.

The necessary power supplies for operating the ion source are powered from a 5 kVA, 160 kV isolation transformer and floated at the source potential which is established by a 0 to 160 kV power supply. The ion beam is extracted by an open cylindrical extractor for efficient vacuum pumping of the source region. The beam is then focused and accelerated to ground potential through a constant gradient acceleration tube.

The beam is mass separated by 15^{o} deflection through a 6 in. diameter electromagnet and collimated to 0.1^{o} by two 0.5 cm diameter apertures spaced 3 m apart. The diameter of the apertures can be readily varied from 1.5 mm to 1 cm if greater or less beam divergence is desired. At the target, which is located 3.5 m from the magnet, 1 amu between mass peaks corresponds to a 2 cm separation for masses around phosphorus (mass 31) and 0.5 cm separation for masses around antimony (mass 122).

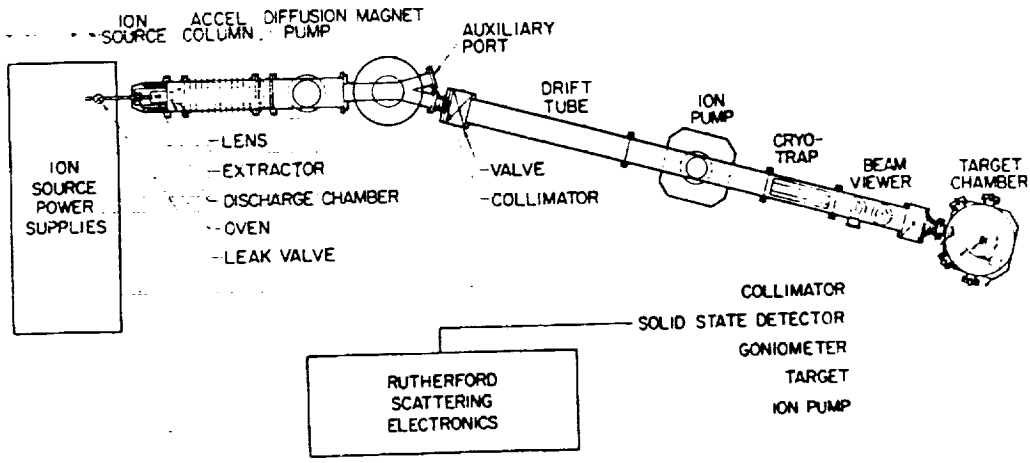

Fig. A-1. Ion channeling research system.

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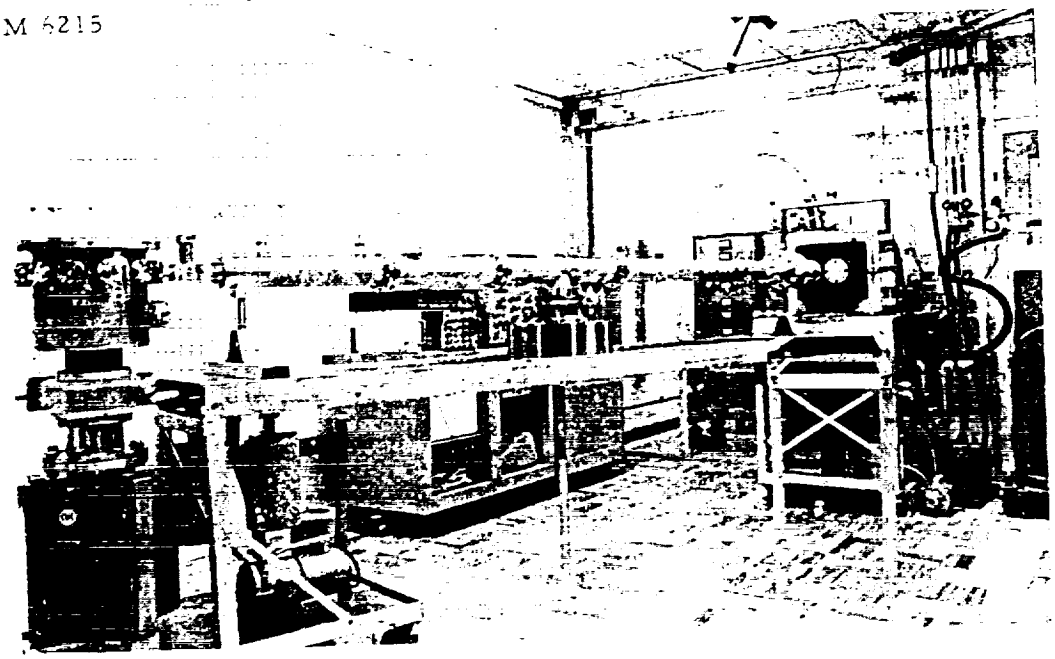

Fig. A-2. Ion channeling research system.

System Characteristics:

Ion species: essentially any in periodic table; employs a Danfysik ion source

Ion energy: 5 to 160 keV

Pumping: Ion pumps at target; trapped diffusion pumps and cryowall at source ~10^{-7} Torr

Beam current: 1 to 100 μA

Mass separation: magnetic

Beam scanning: none

Beam collimation and beam-substrate alignment: 0.1 degree; alignment by Rutherford scattering of protons.

Vacuum pumping of the system is provided by a 1500 liter/sec, cryogenically baffled, diffusion pump at the acceleration tube and by two 200 liter/sec ion pumps, one located at the collimator drift tube and the other at the target chamber. Hydrocarbon contamination of the target by diffusion pump oil vapor is reduced by a cryotrap in the drift tube section before the target chamber. The pressure in the target chamber during implantation is typically 1×10^{-7} Torr.

The system has been aligned and tested with up to 160 keV ion beams of H^+, He^+, and Sb^+. Greater than 1 μA of current of each ion species was delivered to the target. Each ion beam was readily focused to a 3 mm diameter circular spot. The Sb^+ beam gave two spots separated by 1 cm, corresponding to $^{121}Sb^+$ and $^{123}Sb^+$. The observed separation is in agreement with the calculated value.

Target crystal alignment to less than 0.1^o with the beam axis is accomplished using proton backscattering techniques. The protons are produced by introducing hydrogen gas into the ion source so that the proton beam and heavy ion beam are collimated identically. The backscattered protons are detected by a semiconductor nuclear particle detector, and the necessary rotational degrees of freedom of the target are provided by a goniometer driven by stepping motors.

The goniometer is illustrated in Figs. A-3 and A-4. With this instrument the orientation of the crystal sample can be adjusted through a stepping motor drive system controllable from outside the vacuum system. Three independent angular orientations are available. A tilt angle θ about a vertical axis through the target face is introduced through the large horizontal gear which can be seen in the photograph. Rotation in azimuth about a horizontal axis is introduced through the vertical disk to which the crystal is attached. The disk is adjusted in situ by means of the three peripheral screws to permit the introduction of the third independent angular displacement.

The use of stepping motor drive throughout permits highly flexible operation of this instrument. Counters, driven by slave motors, display angular position to within 0.02^o. Stepping rate for the motors of up to a maximum of 80/sec is controllable by the operator in eight speed ranges and two directions. At the maximum stepping rate the entire rotation axes can be traversed in about 4.5 min. The speed is controlled electrically by means of an oscillator which drives a flip-flop, which in turn drives a commercial pulsing circuit designed to operate with the stepping motors. The front plate to which the crystal is attached with fine spring clips is removable, so that changing crystals involves only minimum disturbance to the goniometer.

B. Crystal Alignment

The study of ion channeling in crystalline targets requires accurate alignment (less than 0.1°) of a major crystallographic axis of the crystal with the ion beam. In order to accomplish this alignment, it is necessary to determine the angle between the beam and the crystal axis; i.e., the θ, ϕ coordinates of the axis with respect to the beam. At these settings of θ and ϕ, the beam is then aligned with the crystal axis.

The technique for determining the coordinates of the crystal axis is based on the measurement of the decrease in backscattered proton yield as the major crystal planes are rotated through a proton beam.* For detection of the backscattered protons, a surface barrier detector (15 keV FWHM) is located about 10 cm from the goniometer face, as shown in Fig. A-4. The pulses from the detector are first amplified and then discriminated to remove low energy pulses. They are then counted by a count rate meter whose output is monitored by a strip chart recorder. A 400 channel analyzer in parallel with the count rate meter gives the energy spectrum of the backscattered protons.

The backscattered yield as a function of azimuthal angle ϕ at constant tilt angle $\theta = 3.5^{\circ}$ is shown in Fig. A-5 for 140 keV protons incident on the {111} face of a silicon crystal. The discriminator is adjusted to permit only protons scattered near the surface to be counted. Distinct dips or decreases are observed whenever a major crystal plane is rotated through the beam. The most pronounced dips (~3-1) correspond to {110} planes, and the smaller dips correspond to {112} planes.

A polar coordinate plot showing the {110} planes is given in Fig. A-6; the intersection of these planes locates the <111> axis with respect to the center of rotation, which is aligned with the beam axis. In this case the coordinates of the <111> axis are $\phi = 270^{\circ}$, θ 0 9°. At these settings the beam is aligned with the <111> axis to less than 0.1°. However, in order to tilt through the <111> at various values of ϕ, the front face of the goniometer is adjusted in situ to bring the <111> axis into coincidence with the center of rotation. The dashed lines in Fig. A-6 represent the adjusted positions of the {110} planes, showing that the <111> is at the center of rotation and thus aligned with the beam at $\theta = 0$ for any value of ϕ.

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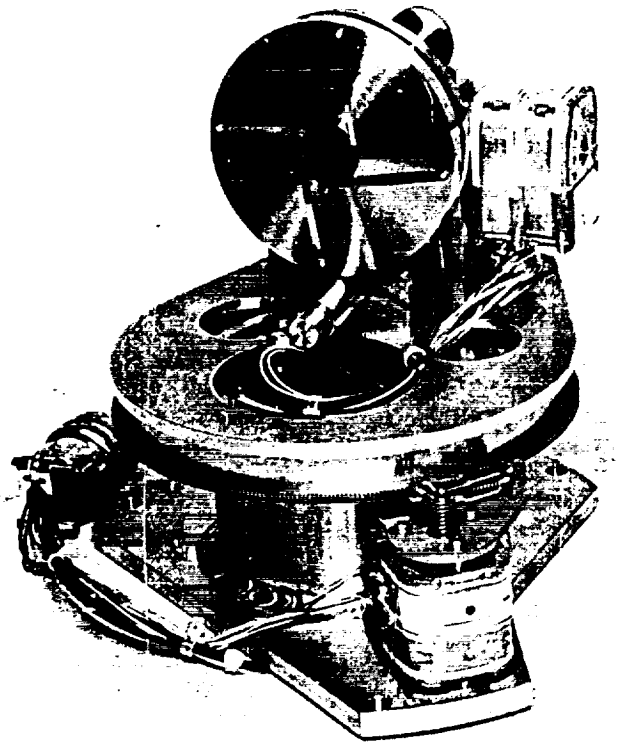

Fig. A-3. Crystal goniometer constructed for use with the channeling apparatus.

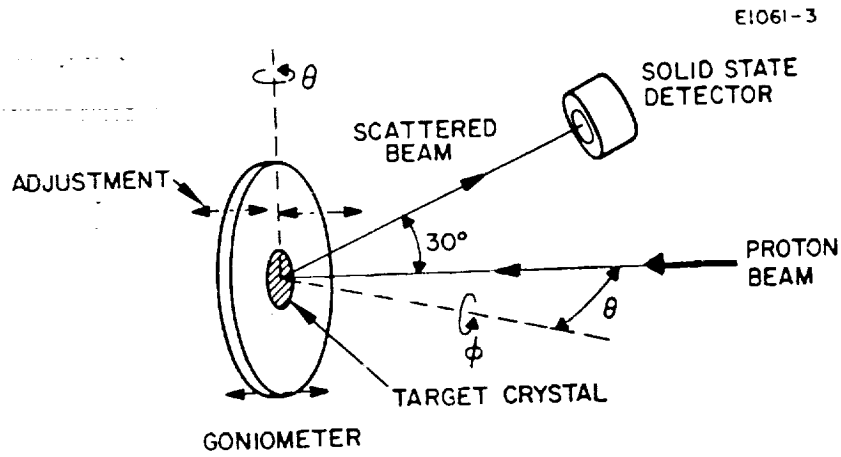

Fig. A-4. Schematic of scattering assembly used for backscattering analysis and alignment of the target crystal.

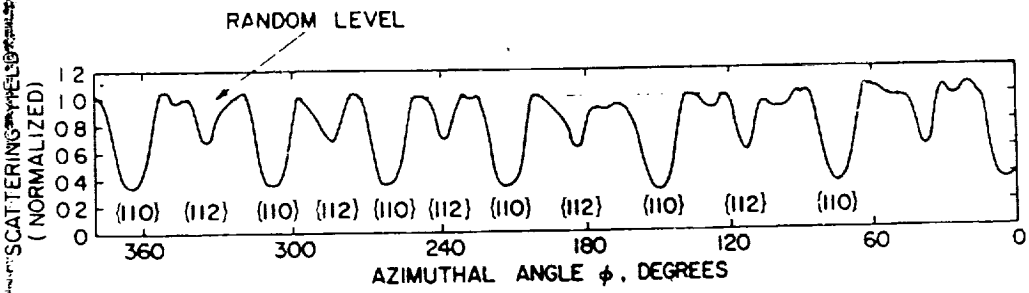

Fig. A-5. Scattering yield as a function of ϕ at constant $\theta = 3.5^{\circ}$ for 140 keV protons incident on the {111} face of silicon. The major planar dips are indicated.

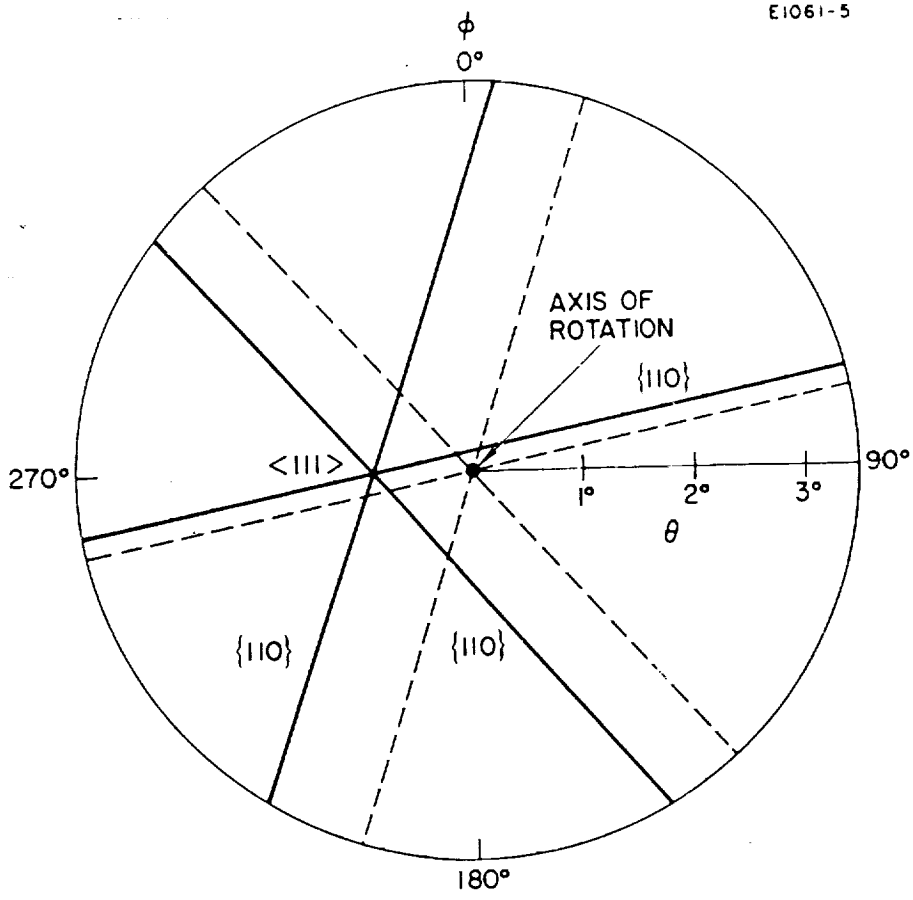

Fig. A-6. Polar coordinate plot of the data in Fig. A-5 showing the {110} planes (solid lines). The intersection of the planes determines the coordinates of the <111> direction ($\phi = 270^{\circ}$, $\theta = 0.9^{\circ}$). The dotted lines represent adjusted positions of the {110} planes showing that the <111> is at the center of rotation O.